Zynq-7000 All Programmable SoC ZC702 Evaluation Kit

Getting Started Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/25/2012	1.0	Initial Xilinx release.
05/29/2012	1.1	Added Figure 4-3 and the text just before and after it.
06/21/12	1.2	Chapter 1, Introduction: Added a "Reference Designs and Demonstrations" group to section ZC702 Evaluation Kit Contents, page 6. Changed cable from Digilent USB JTAG to Digilent USB-to-JTAG. Added that the SD MMC card contains bootable configuration files for the Base TRD demo design files and Linux applications platform. Updated USB JTAG interface information and added details to the clock sources list in section Key Features, page 7. Changed FMC1 and FMC2 connector types to LPC I/O expansion connectors. Added tables of default settings to the section Default Jumper and Switch Settings, page 9. Chapter 2, Zynq-7000 All Programmable SoC ZC702 Evaluation Kit Built-In Self-Test: Updated switch settings in the Introduction, page 13. Added bring-up details through the chapter. Settings were added to section Run the BIST Application, page 19. Added Chapter 3, Getting Started with the Base Targeted Reference Design. Added Chapter 4, Evaluating the AMS101 Evaluation Card. Additional references were added through the book and to Appendix A, Additional Resources.
09/21/12	1.2.1	Updated title.

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Appendix B: Warranty

Introduction

Overview

The ZC702 Evaluation kit shown in Figure 1-1 is based on the XC7Z020 CLG484-1 All Programmable SoC device. For additional information, see the Zynq™-7000 All Programmable SoC Family Product Table [Ref 1]. (See Appendix A, for references.) A built-in self-test (BIST) is provided for the ZC702 Evaluation kit. The BIST provides a convenient way to test many of the board's features on power-up. The tutorials and reference designs available on the ZC702 product page can be used to further explore the capabilities of the ZC702 board and the Zynq-7000 All Programmable SoC [Ref 2]. For the most up-to-date information on the content provided with the ZC702 Evaluation kit, see the ZC702 product page [Ref 3]. UG873, *Zynq-7000 Concepts, Tools, and Techniques Guide* shows the basic hardware and software flow using the ZC702 board [Ref 4]. The Zynq-7000 All Programmable SoC documentation page is also helpful [Ref 5].

Figure 1-1: **ZC702 Evaluation Kit**

This user guide also describes a Base Targeted Reference Design (TRD) based on Zynq-7000 All Programmable SoC architecture. The Base TRD showcases various features and

capabilities of the Zynq Z-7020 All Programmable SoC for the embedded domain in a single package. TRDs are key components of the Xilinx Targeted Design Platform (TDP) strategy. TDPs from Xilinx provide customers with basic scalable design platforms for the creation of FPGA-based solutions in a wide variety of applications and industries.

ZC702 Evaluation Kit Contents

The ZC702 Evaluation kit includes the following items:

- ZC702 evaluation board featuring the XC7Z020 CLG484-1
- Agile Mixed Signal (AMS) evaluation board
- Full seat ISE® Design Suite Embedded Edition design tools
  - Device-locked to the Zynq-7000 XC7Z020 CLG484-1 device
- Board design files
  - Schematics
  - Board layout files
  - Bill of materials
- Documentation
  - *Getting Started Guide* (this document)
  - Hardware user guide (UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [Ref 6])
  - TRD user guide (UG925, *Zynq-7000 All Programmable SoC ZC702 Base Targeted Reference Design User Guide* [Ref 7])
- Reference Designs and Demonstrations
  - BIST Utility and Demonstration
  - Targeted Reference Design (TRD), demonstrating a video processing pipeline.

    Note: The video demonstration contains the licensed IPs with no timeout. To recompile this design, the user needs to register for an evaluation IP license for the Video IP.
  - AMS demonstration, providing an overview of the analog capabilities of the Zynq-7000 All Programmable SoC devices.
- 12V AC adapter power supply
- Cables
  - RJ-45 Ethernet cable
  - HDMI™ cable

  - USB Type-A to USB Micro-B cable (Digilent USB-to-JTAG Programing Port)
  - USB Type-A to USB Mini-B cable (serial UART)
- USB flash drive (contains reference design, documents, and board source files)
- Secure Digital Multimedia Card (SD MMC) (contains bootable configuration files for the Base TRD demonstration design files and Linux applications platform)

The kit contains the software and reference designs, a demonstration, and documents to help the user get started quickly.

Key Features

Key features of the ZC702 evaluation board include:

- Zynq-7000 XC7Z020-1CLG484 device
- 1 GB DDR3 component memory (four 256 Mb x 8 devices)
- 128 Mb Quad SPI flash memory
- USB 2.0 ULPI (UTMI+ low pin interface) transceiver
- SD MMC connector
- USB JTAG interface through the Digilent USB-to-JTAG programing port
- Clock sources:
  - Fixed user clock—(200 MHz) LVDS oscillator (differential)
  - Programmable user clock—I2C programmable (10 MHz to 810 MHz, with a default setting of 156.250 MHz) LVDS oscillator (differential)
  - Zynq processor reference clock—Fixed (33.33 MHz) LVCMOS oscillator (single-ended)
- Ethernet PHY RGMII interface with RJ-45 connector
- 10/100/1,000 tri-speed Ethernet PHY
- USB-to-UART bridge
- HDMI codec
- I2C bus
- I2C bus multiplexed to:
  - Si570 user clock
  - ADV7511 HDMI codec
  - M24C08 EEPROM (1 KB)

  - 1-to-16 TCA6416APWR port expander
  - RTC-8564JE real-time clock
  - FMC1 LPC I/O expansion connector
  - FMC2 LPC I/O expansion connector
  - PMBUS data/clock
- Status LEDs:
  - Ethernet status
  - Power good
  - FPGA INIT
  - FPGA DONE
- User I/O:
  - Eight user LEDs
  - Two user pushbuttons
  - Two user switches (2-position DIP switches)
- CPU reset pushbutton
- Two VITA 57.1 FMC LPC connectors
- Power on/off slide switch
- Power management with PMBus voltage and current monitoring through TI power controllers
- XADC header with access to dual 12-bit 1 MSPS XADC port
- (SW1 – POR_B) boot configuration options:
  - SD MMC Boot mode
  - Quad SPI flash memory
  - USB JTAG configuration port (Digilent module)
  - Platform cable header JTAG configuration port

For more detailed information about ZC702 board features, peripheral devices, and pinouts, see the hardware user guide UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [Ref 6].

Default Jumper and Switch Settings

Figure 1-1 calls out the major features on the ZC702 board. See UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [Ref 6] for more detailed information about the ZC702 board.

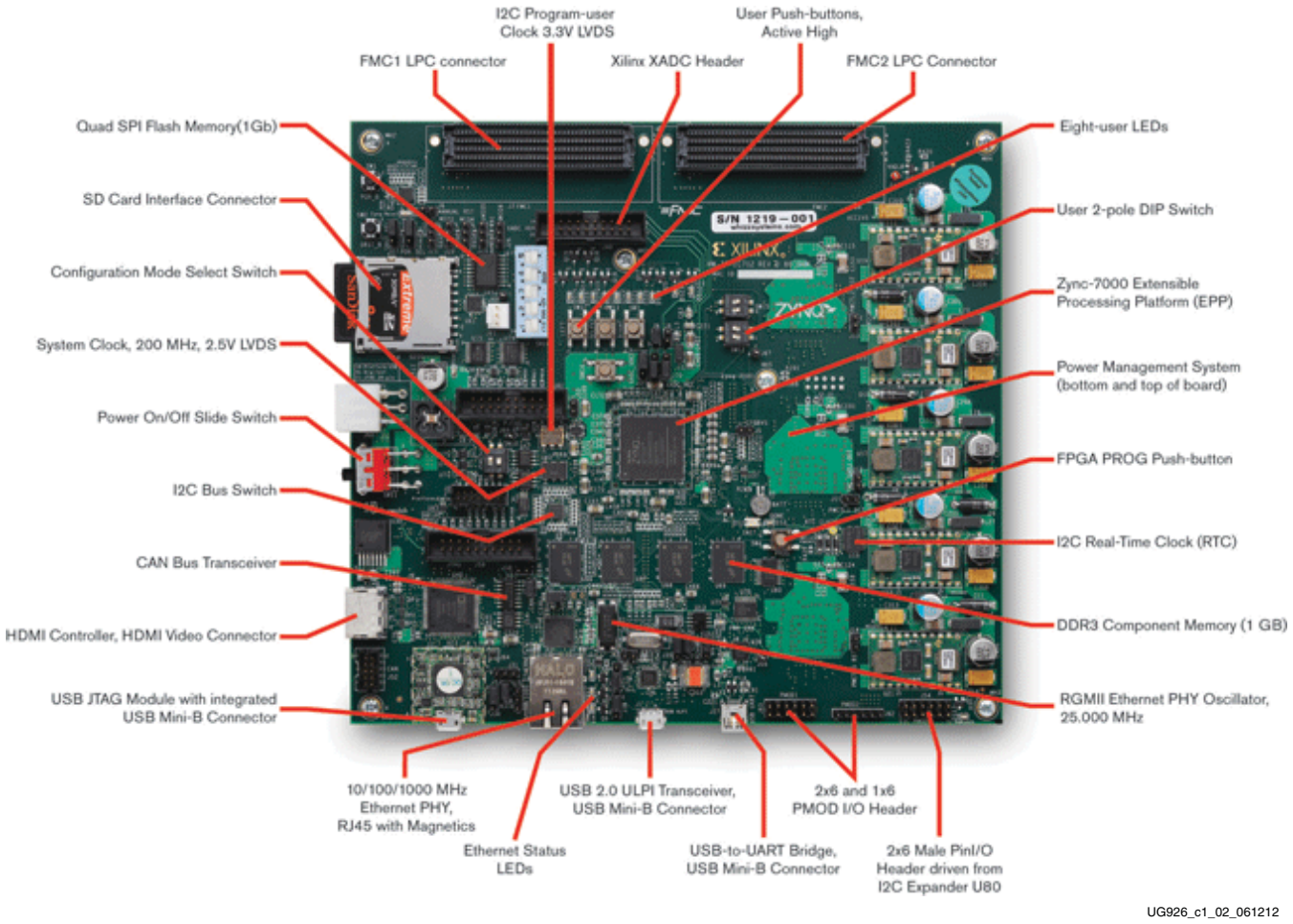

Figure 1-2: **Feature Callout for the ZC702 Board**

Default factory settings of jumpers and switches on the ZC702 board are highlighted in Figure 1-3. Default switch and jumper settings are listed in Table 1-1 and Table 1-2.

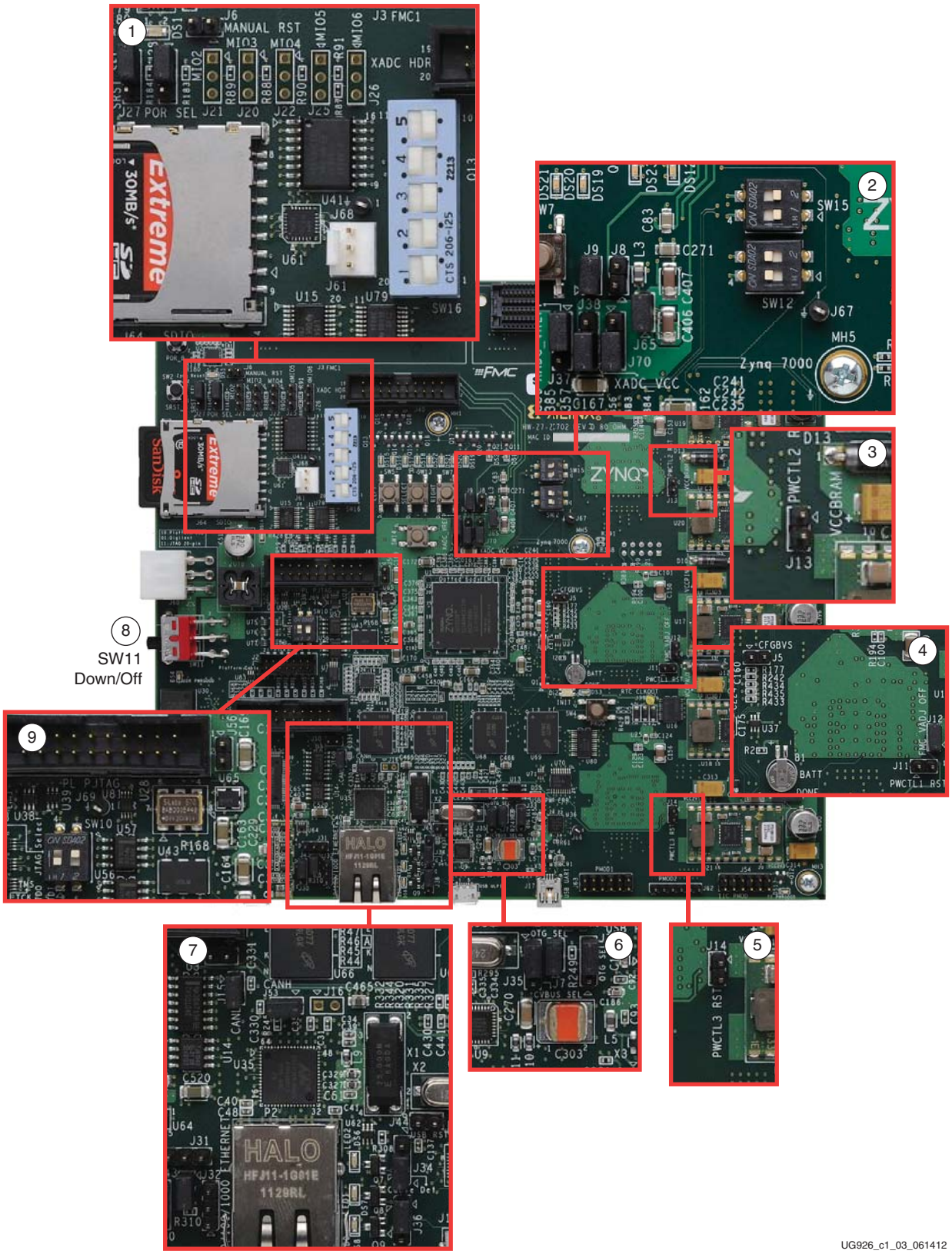

Figure 1-3: **Default Jumper and Switch Settings on the ZC702 Board**

Table 1-1: **Default Switch Settings**

Switch	Position	Setting	Figure 1-3 Callout
SW10 (JTAG chain input select two-position DIP switch)	1	Off	9
	2	On	
SW12 (two-position DIP switch)	1	Off	2
	2	Off	
SW15 (two-position DIP switch)	1	Off	2
	2	Off	
SW16 (five-position DIP switch)	1	Right	1
	2	Right	
	3	Right	
	4	Right	
	5	Right	
SW11 (power slide switch)		Off	8
	1	Down	

Default jumper positions are shown in Figure 1-3 and listed in Table 1-2.

Table 1-2: **Default Jumper Settings**

Jumper	Function	Default Position	Figure 1-3 Callout
HDR_1 X 2			
J5	CFGBVS short to GND	OFF	4
J6	POR Master Reset	OFF	1
J7	USB 2.0 USB_VBUS_SEL	1-2	6
J8	XADC GND L3 Bypass	OFF	2
J9	XADC GND	ON	2
J10	ARM HDR J41 pin 2 to VADJ	OFF	7
J11	UCD9248 U32 ADDR52 RESET_B	OFF	4
J12	FMC_VADJ_ON_B	ON	4
J13	UCD9248 U33 ADDR53 RESET_B	OFF	3
J14	UCD9248 U34 ADDR54 RESET_B	OFF	5
J15	CAN BUS COMMON-MODE CANH HDR	1-2	7
J43	Ethernet PHY HDR	1-2	7
J44	USB 2.0 USB_RESET_B	OFF	7
J53	CAN BUS COMMON-MODE CANL HDR	1-2	7
J56	JTAG HDR J58 pin 2 3.3V SEL	OFF	9
J65	XADC_VCC5V0 = VCC5V0	OFF	2

Table 1-2: **Default Jumper Settings *(Cont'd)***

Jumper	Function	Default Position	Figure 1-3 Callout
HDR_1 X 3			
J27	PS_SRST_B	1-2	1
J28	PS_POR_B	1-2	1
J30	Ethernet PHY HDR	1-2	7
J31	Ethernet PHY HDR	NONE	7
J32	Ethernet PHY HDR	NONE	7
J33	USB 2.0 Mode	2-3	6
J34	USB 2.0 J1 ID SEL	1-2	7
J35	USB 2.0 J1 VBUS CAP SEL	1-2	6
J36	USB 2.0 J1 GND SEL	1-2	7
J37	XADC_VREP SEL	1-2	2
J38	XADC_VCC SEL	2-3	2
J70	XADC_VREF Source SEL	2-3	2

Zynq-7000 All Programmable SoC ZC702 Evaluation Kit Built-In Self-Test

Introduction

The BIST tests many of the features offered by the Zynq-7000 All Programmable SoC ZC702 Evaluation kit. The test is stored in the onboard nonvolatile Quad SPI flash memory, and configures the All Programmable SoC when the mode switch SW16 is set to where SW1, 2, 3, and 5 are switched to the right and SW4 is switched to the left.

indicating QSPI configuration. This exercise of running the BIST demonstration should take approximately 10 to 15 minutes.

Note: For a description of all the features on the ZC702 board, see UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [Ref 6].

BIST Setup Requirements

These are the prerequisites for running the BIST demonstration.

- Hardware setup:
  - ZC702 evaluation board with XC7Z020 CLG484-1 part
    - A power adaptor and power cable for the ZC702 board
  - USB Type-A to Mini-B cable (for UART)
  - AC power adapter (12 VDC)
- Windows software and driver setup:
  - TeraTerm Pro (or similar) terminal program (might already be installed)
  - USB-UART driver from Silicon Labs [Ref 8] (might already be installed)

Hardware BIST Board Setup

This section describes the hardware setup and use of the terminal program for running the BIST application. It contains step-by-step instructions for board bring-up.

ZC702 Evaluation Board Setup

The default jumper and switch settings of the ZC702 board are shown in Figure 1-3, Table 1-1, and Table 1-2.

1. Set the SW16 switch as shown in Figure 2-1, where SW1, 2, 3, and 5 are switched to the right and SW4 is switched to the left for the BIST to boot from Quad SPI device and run the system demonstration utility.

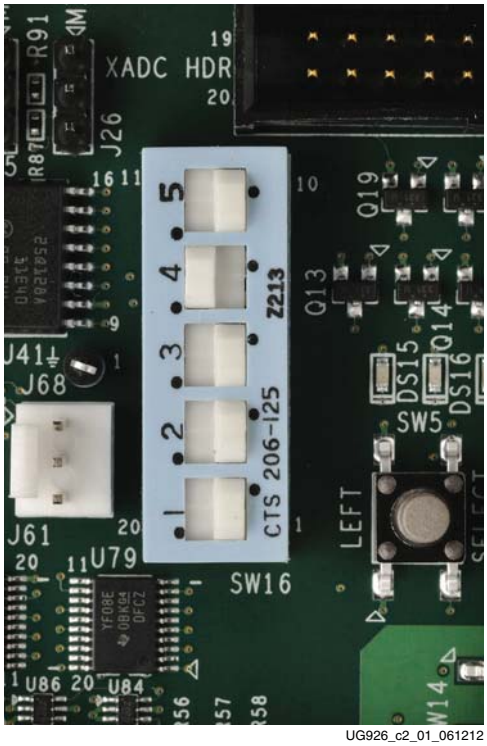

Figure 2-1: **Settings for the Mode Switch to Boot from Quad SPI Mode**

Hardware Bring-Up

This section describes the steps for hardware bring-up.

1. Be sure to have the SW16 Mode switch settings set to those shown in Figure 2-1.

2. With the ZC702 board switched OFF (SW11 in the down position, as shown in Figure 1-3), plug the USB Mini-B cable into the Mini USB port J17 labeled USB UART on the ZC702 board and the other end into a open USB port on your PC (see Figure 2-2).

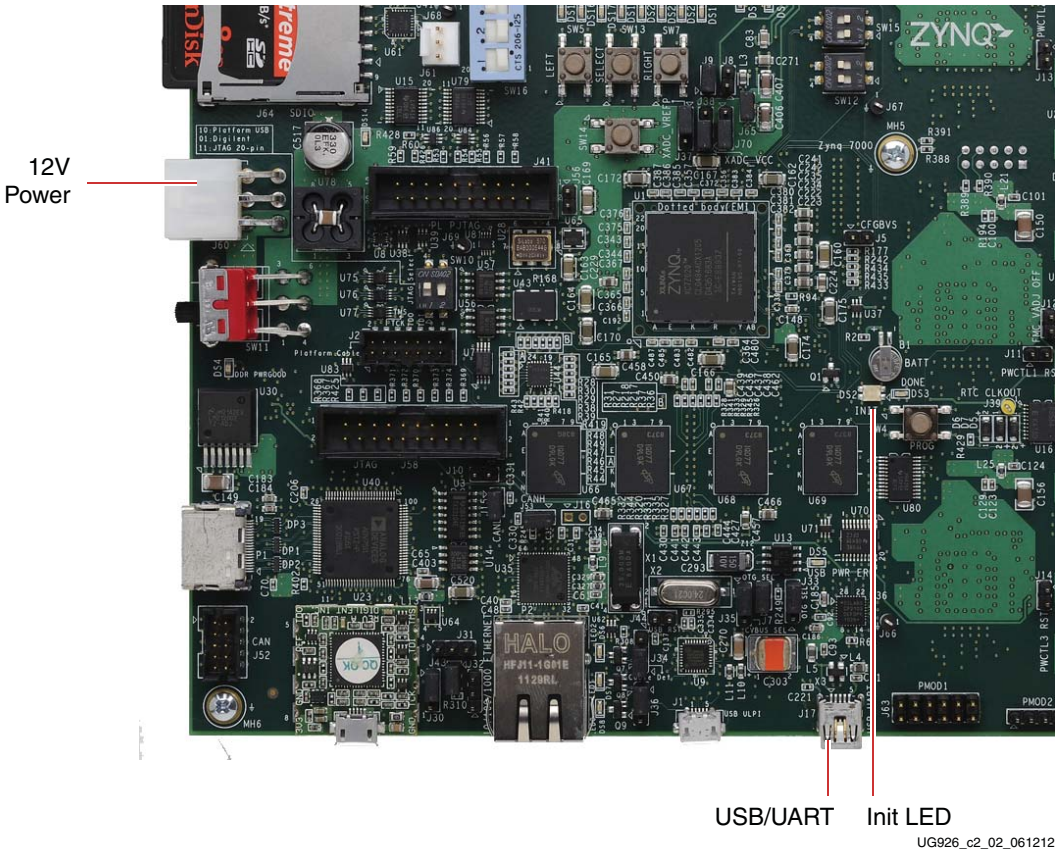

Figure 2-2: **ZC702 with the UART and Power Cable Attached**

3. Connect the power cable.
4. Switch the ZC702 board's power to ON (SW11 switched up as shown in Figure 1-3).

Install the USB-UART Driver

1. Run the downloaded executable UART-USB driver file, listed in BIST Setup Requirements, page 13. Running the executable file enables USB-to-UART communications with a host PC.

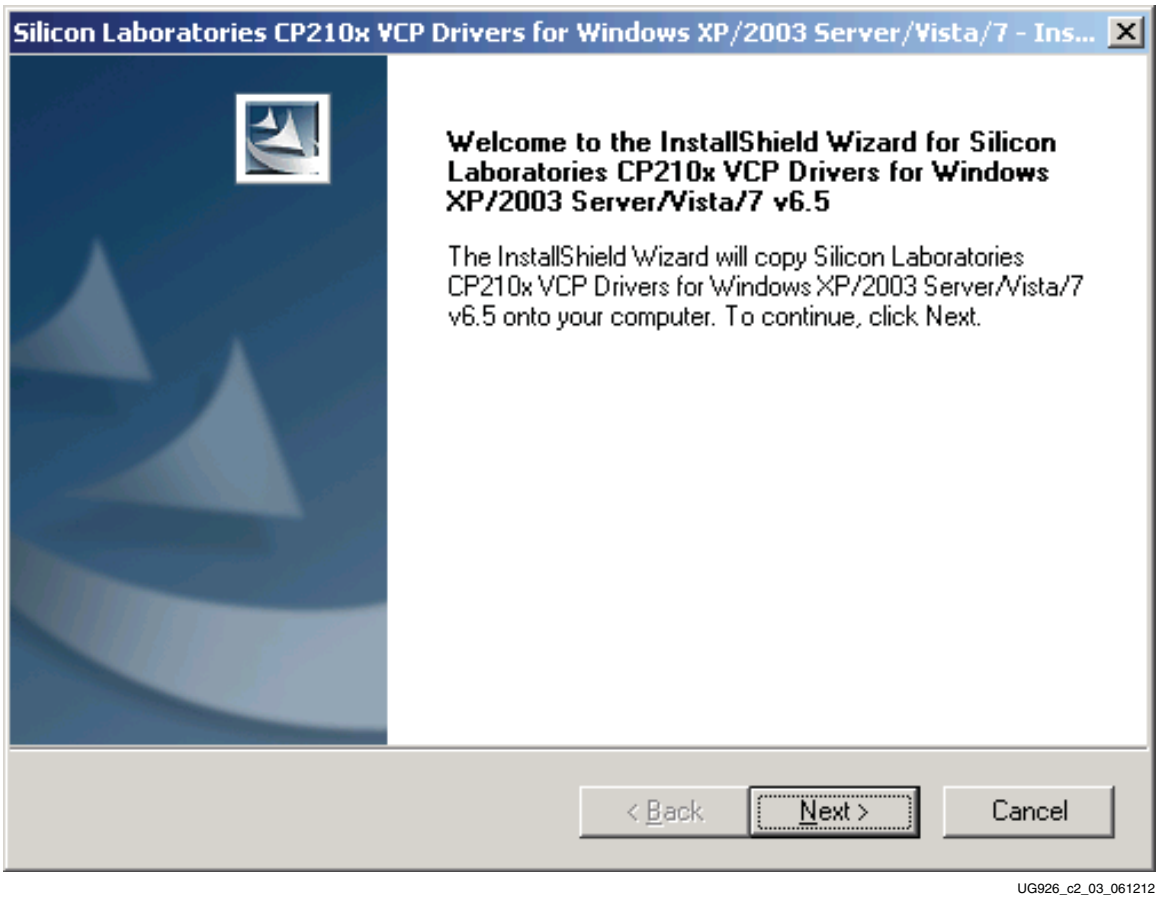

Figure 2-3: **UART Cable Driver Installation**

2. Set the USB-UART connection to a known COM Port and baud rate in the Device Manager.
   a. Right-click **My Computer** and select **Properties**.
   b. Select **Device Manager** on the left side. (On Windows XP, select the **Hardware** tab and then the **Device Manager** button.
   c. Right-click the **Silicon Labs** device in the list and select **Properties.**
   d. Click the **Port Settings** tab. Click the **Advanced...** button.
   e. Select an open COM port between COM1 and COM4. This allows the computer to remember the assignment and not reassign it each time the board serial UART port is plugged in.
   f. Select the baud rate = **115200**, Data bits = **8**, Parity = **None**, Stop Bits = **1**, and Flow control = **None.** Click **OK**.

   Note: Steps and diagrams refer to using a Windows XP or Windows 7 host PC.

Figure 2-4 through Figure 2-6 show the steps for setting the USB-UART port.

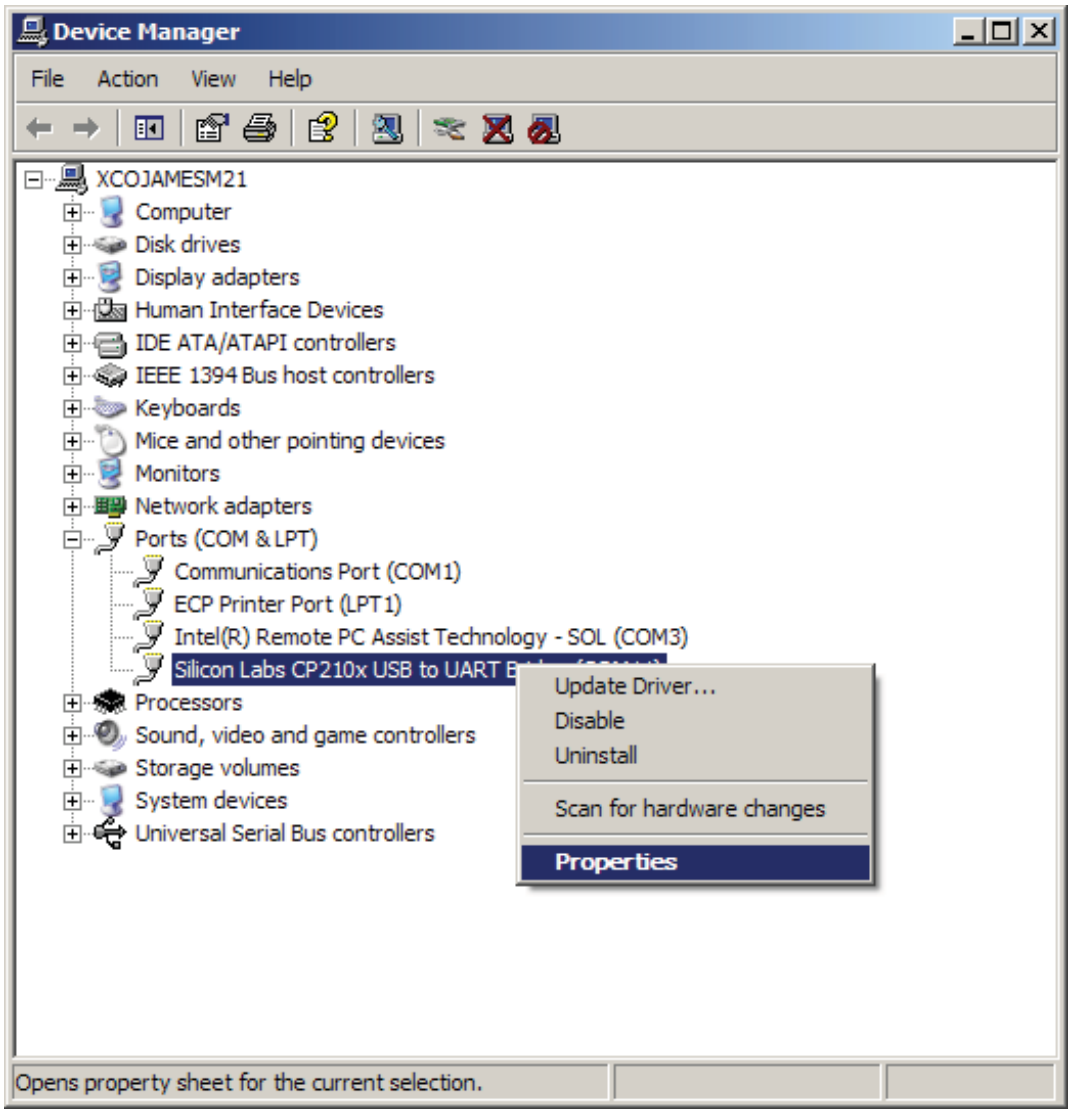

Figure 2-4: **Configuring the Driver**

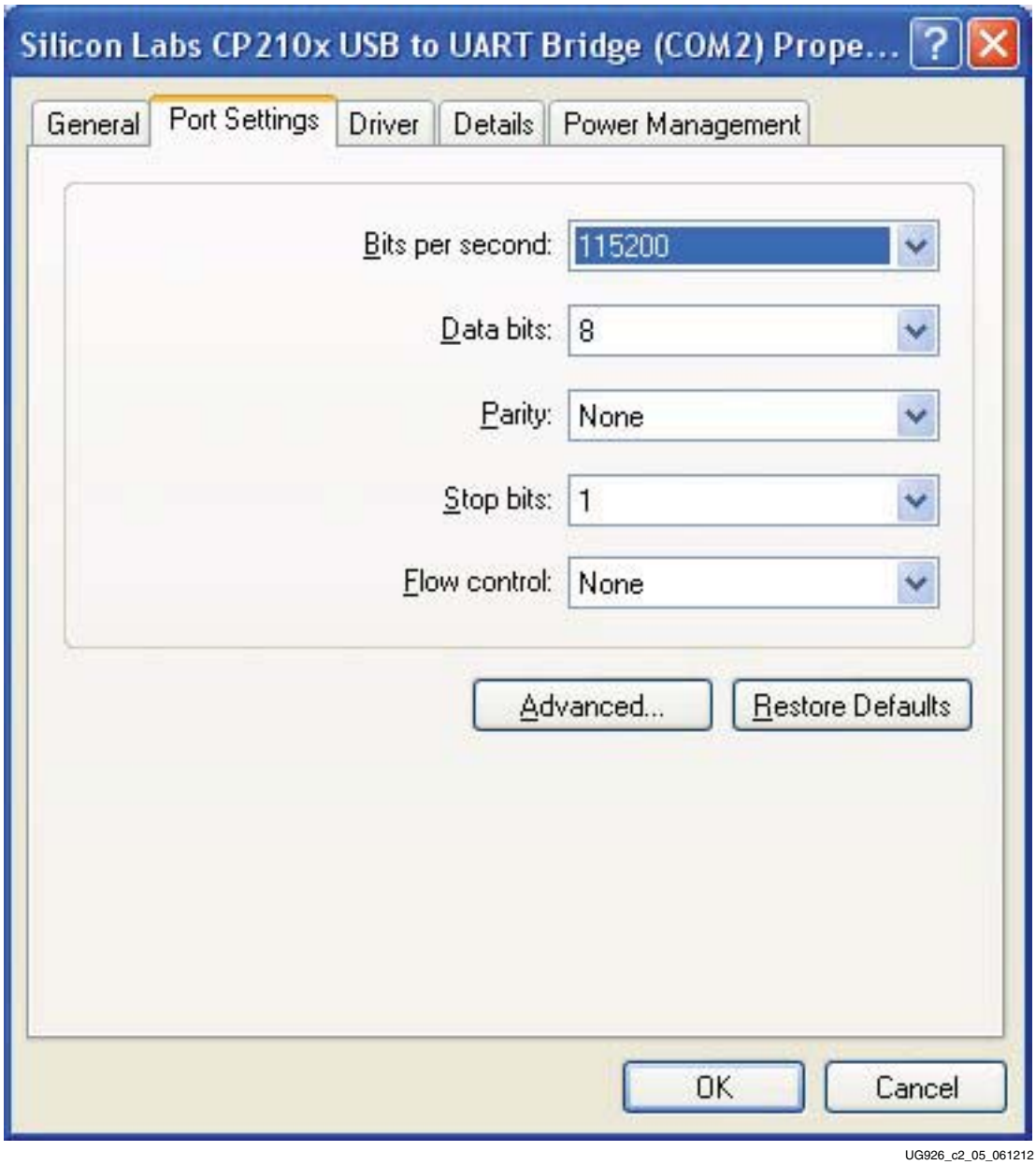

Figure 2-5: **UART Port Setting Tab**

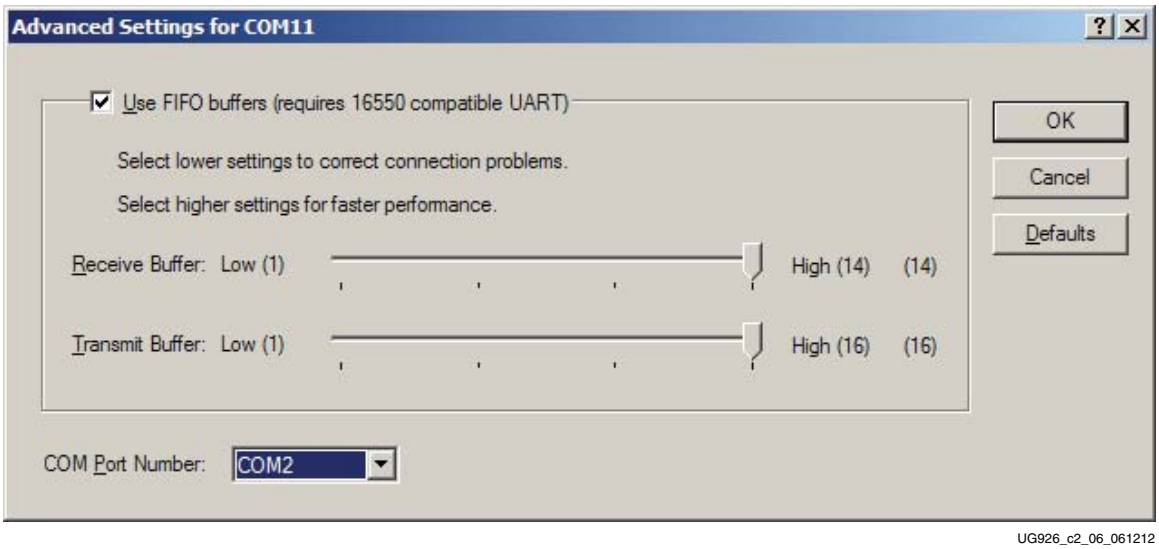

Figure 2-6: **Select a COM Port (between COM1 and COM4)**

Run the BIST Application

1. Start Tera Term or a comparable installed terminal program. Configure it to have the following settings:
   Baud = **115200**, Data = **8**, P = **None**, Stop = **1** and Flow = **None**.
2. Press POR_B (SW1) located in the top left corner of the ZC702 board and view the BIST output on the terminal window (see Figure 2-7).

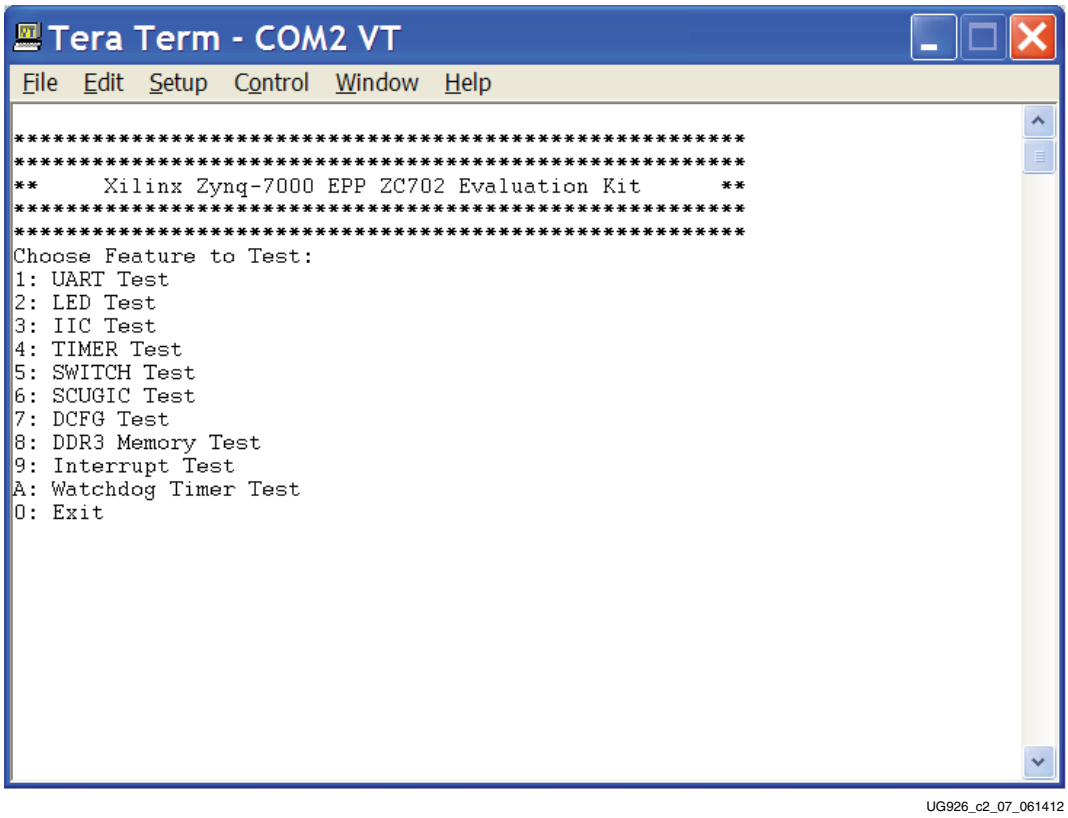

Figure 2-7: **BIST Main Menu**

3. Select each relevant test and observe the test results.

For more information on the BIST software and additional tutorials, including how to restore the default content of the onboard Quad SPI flash nonvolatile storage, see the ZC702 resource page [Ref 3].

For more detailed information about these BIST tests, refer to UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide* [Ref 6]. Also refer to the ZC702 BIST User Guide found in the **Docs & Designs** tab on www.xilinx.com/zc702 [Ref 3] i.e., the ZC702 BIST PDF file, XTP180.

If any of the BIST tests fail, check the settings of the switches and jumpers as shown in Figure 1-3, Table 1-1, and Table 1-2. If these settings are correct and the test still fails, please contact Xilinx Support and open a WebCase.

Getting Started with the Base Targeted Reference Design

Introduction

Figure 3-1 shows the system block diagram for Zynq-7000 All Programmable SoC Base TRD.

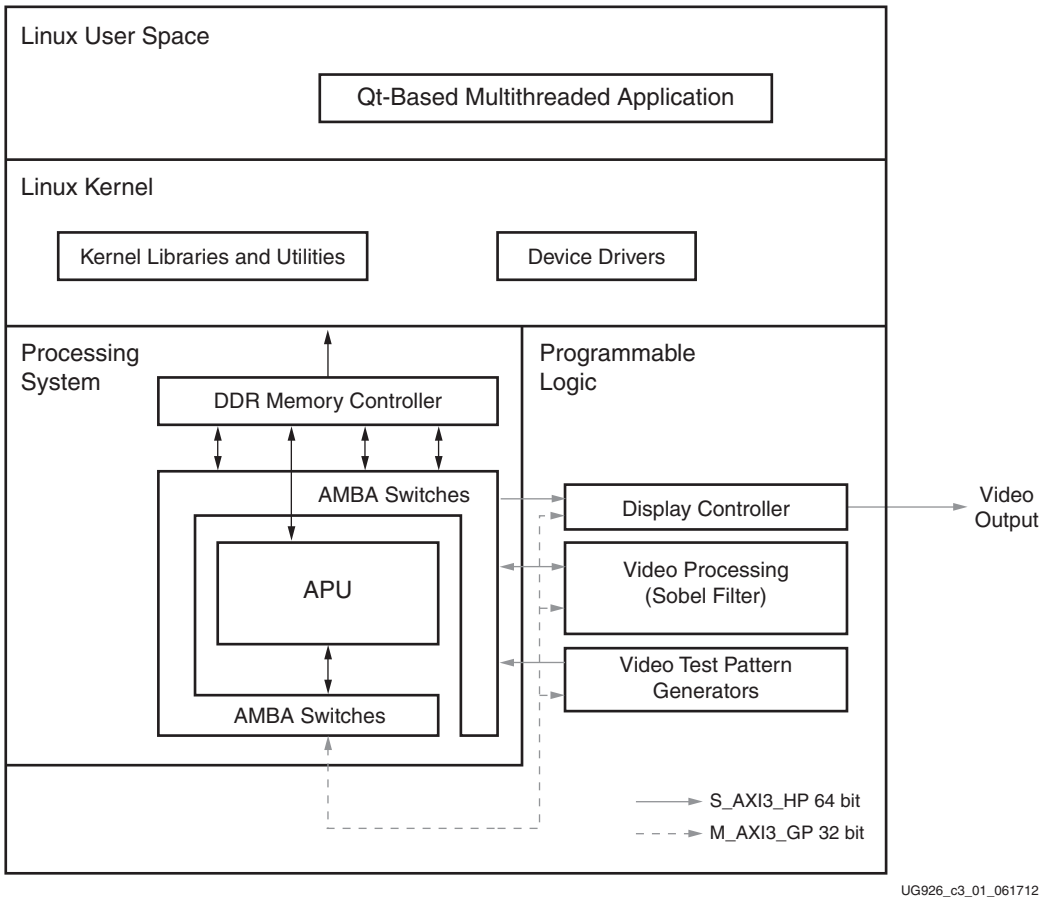

Figure 3-1: **Zynq-7000 All Programmable SoC Base TRD System Block Diagram**

The Base TRD showcases various features and capabilities of the Zynq Z-7020 All Programmable SoC device for the embedded domain in a single package. The Base TRD consists of two processing elements: The Zynq-7000 All Programmable SoC PS and an

interconnect logic-based video accelerator. The All Programmable SoC allows the user to implement a specific functionality either as a software program running on the Zynq-7000 All Programmable SoC PS or as a hardware design inside the PL. The Base TRD demonstrates how the user can seamlessly switch between a software or a hardware implementation, contributing to ease of use. The TRD also demonstrates the value of offloading computation-intensive tasks onto PL, thereby freeing the CPU resources to be available for user-specific applications.

This section of the document provides step by step instructions for bringing up the board and for running a video demonstration out of the box.

The ZC702 Evaluation kit comes with an SD card loaded with binaries that enable the user to run the video demonstration and software application. It also includes the binaries necessary to configure and boot the Zynq-7000 All Programmable SoC board.

Note: The screen captures in this document are conceptual representations of their subjects and provide general information only.

Base TRD Key Features

The PS includes:

- Two ARM Cortex-A9 MPcore processors, each with a 32 KB instruction cache, a 32 KB data cache, and a NEON™ media processing engine and vector floating-point processor (VFPv3).
- 512 KB of level 2 cache
- 256 KB of on-chip RAM
- ARM AMBA® AXI interconnect
- Multi-protocol, 32-bit DDR DRAM controller
- 1 GB DDR3 running at 533 MHz
- Standard peripheral interfaces including USB, Ethernet, UART, I2C, SD MMC, and GPIO
- Clocks and reset for PL
- High bandwidth interconnect between PS and PL

The PL includes:

- Two AXI interconnects, 64-bit wide at 150 MHz
- One AXI interconnect, 32-bit wide at 75 MHz
- AXI VDMA(s)
- A full HD video input and output interface

- A Sobel accelerator
- Two AXI Performance Monitors

The software includes:

- Xilinx Zynq-7000 All Programmable SoC standard Linux kernel (based on Open Source Linux version 3.x)
- Linux device drivers for TRD-specific IPs.
- A Qt-based Linux application demonstrating the video processing pipeline
- A command line menu-based Linux application demonstrating the video processing pipeline

Note: The video demonstration contains the licensed IPs with no timeout.

Base TRD Hardware Setup Requirements

These items are required to run and test the Base TRD and the video demonstration:

- The ZC702 evaluation board with the XC7Z020 CLG484-1 part
- USB Type-A to USB Mini-B cable (for UART communications) and a Tera Term Pro (or similar) terminal program
- USB-UART drivers from Silicon Labs [Ref 8]
- AC power adapter (12 VDC)
- An HDMI cable
- SD MMC flash card containing TRD binaries formatted with FAT32

  Note: The included SD MMC is pre-loaded with required binaries. The binaries are loaded into the first partition of the SD MMC card and include:

  - `BOOT.bin`
  - `devicetree.dtb`
  - `zImage`
  - `ramdisk8M.image.gz`
  - `qt_lib.img`
  - `init.sh`
  - `run_sobel.sh`
  - `sobel_cmd`
  - `sobel_qt`
  - `zynq.png`

- A USB Micro-B to female A adaptor with USB hub is needed for connecting a keyboard and a mouse (not included with the kit)
- USB mouse and keyboard (not included with the kit)
- A display monitor that supports full HD resolution: 1920 x 1080p @ 60 Hz (not included with the kit)

  Note: The example mentioned in this package has been tested with a Dell model #P2412H display monitor. However, the example should work well with any HDMI-compatible output device.

TRD Demonstration Procedure

This section provides a procedure for setting up the ZC702 board and running the demonstration provided with the kit.

Board Setup

1. Connect the cables as shown in Figure 3-2 to prepare the ZC702 board to run the TRD video demonstration.

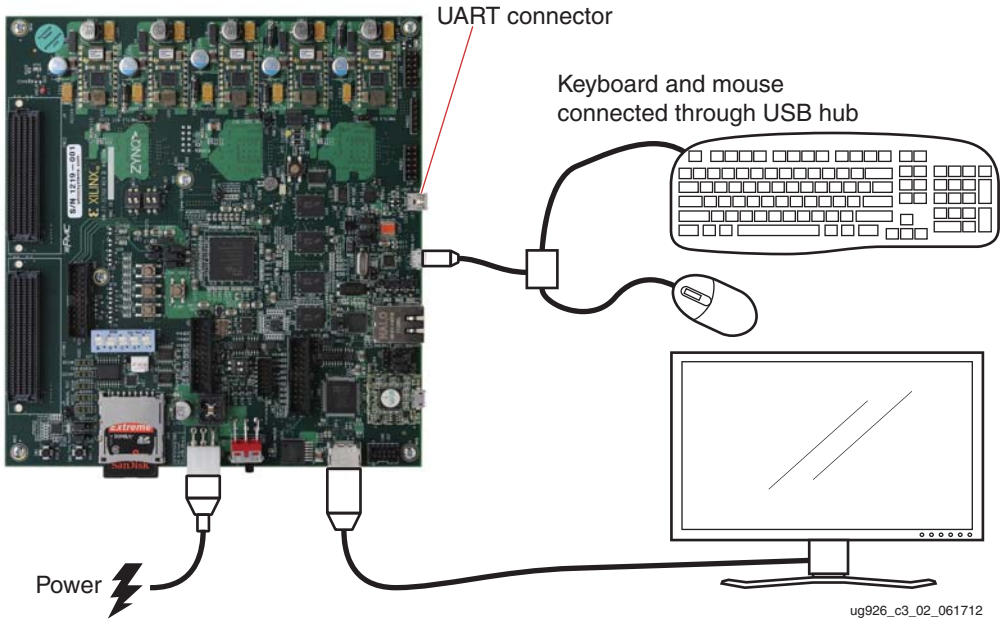

Figure 3-2: **ZC702 Board Setup for a Video Demonstration**

   a. Connect an LCD monitor to the HDMI out port of the ZC702 board using an HDMI cable.

   b. Connect a keyboard and mouse to the USB hub, which is connected to the ZC702 board Micro-B USB connector.

Note: The USB Micro-B to female A adaptor cable and USB hub are not included in the kit.

c. Connect the USB Mini-B cable into the Mini USB port J17 labeled **USB UART** on the ZC702 board and the USB Type-A cable into an open USB port on the host PC for UART communications.

d. Connect the power supply to the ZC702 board. Do not switch the power on.

2. Insert the SD MMC, which contains the TRD binaries, into the SD slot on the ZC702 board.

   Note: If the evaluation kit design files were downloaded online, copy the entire folder `zynq_base_trd_14.x/sd_image` onto the primary partition of the SD-MMC card (which is formatted as FAT32) using an SD-MMC card reader. The files in the SD-MMC card should match the list described in SD MMC flash card containing TRD binaries formatted with FAT32, page 23.

3. Make sure the switches are set as shown in Figure 3-3, which allows the ZC702 board to boot from the SD-MMC card.

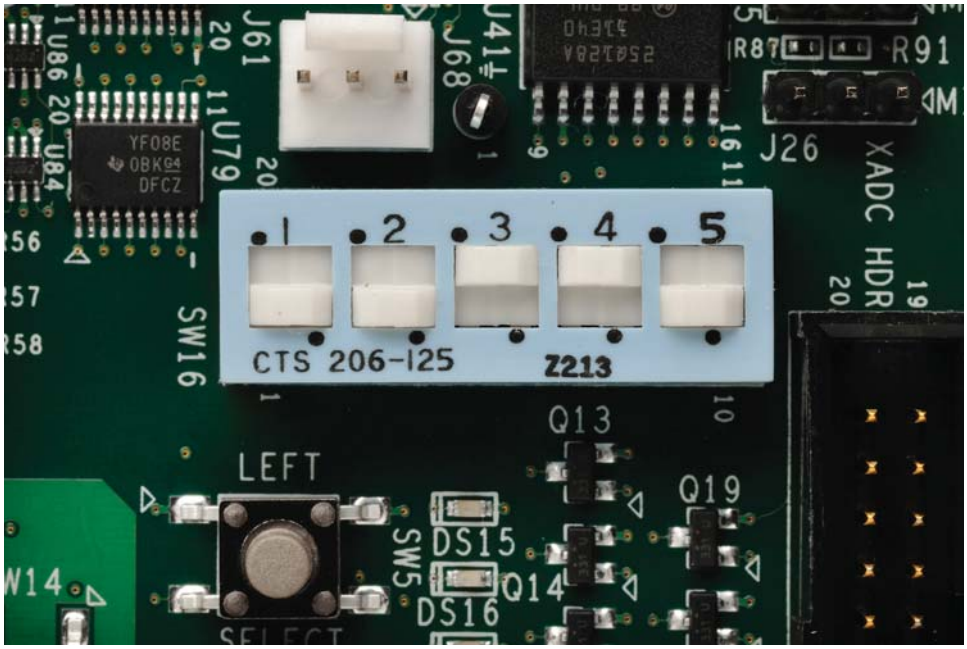

Figure 3-3: **Switch Settings for the Mode Switch to Boot from the SD-MMC Card**

4. Make sure the monitor is set for HDMI or DVI 1920x1080.

Running the Qt-Based GUI Application Demonstration

1. Power on the ZC702 board.
2. Start the installed UART terminal program on your host PC (e.g., Tera Term on a Windows PC, GtkTerm on a Linux PC).

   Use the following UART configuration: Baud rate = **115200**, bits = **8**, parity = **none**, and stop bits = **1**.

   Note: This step is required to view debug information or to run the UART Menu-Based Demonstration application.
3. Wait for the ZC702 board to be configured and booted with Linux. The `zynq>` prompt displays on the monitor screen (approximately 2 minutes). After this, a XILINX ZYNQ banner displays on the LCD screen, as shown in Figure 3-4.

Figure 3-4: **Zynq Linux Command Prompt**

4. The Qt-based video demonstration application starts. The GUI application shows up at the far right of the monitor (see Figure 3-5).

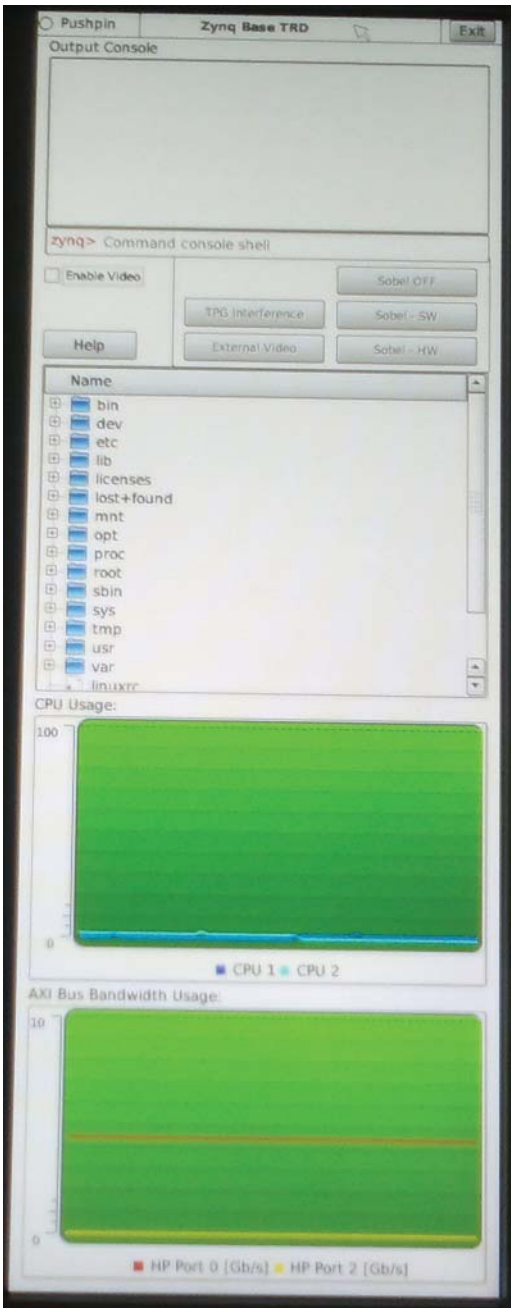

Figure 3-5: **Qt-Based GUI to Control the Video Pipeline**

5. The Qt-based application allows the user to experience the Base TRD video demonstration and is controlled through the mouse. The Qt application window automatically disappears when not in use, but can be re-activated by moving the mouse. To prevent the window from disappearing, the user can click **Pushpin**, which will pin down the control console so that it will not disappear regardless of the mouse position. The user can click **Help** for short messages and information about the control window of the QT application.

6. Click **Enable Video** to start the internal test pattern generator which displays on the monitor.
7. Exercise different options by pressing the buttons available in the GUI to evaluate the different use cases mentioned in Table 3-1.

Table 3-1: **Zynq-7000 All Programmable SoC Base TRD Video Demonstration Use Cases**

Use Case	TPG Control	Sobel Filter Control
1	TPG Pattern	Sobel OFF
2	TPG Pattern	Sobel - SW
3	TPG Pattern	Sobel - HW

Sobel Filter modes are explained as follows:

Sobel OFF

- No processing done. Sobel filter is bypassed.

Sobel – SW

- Video processing (edge-detection filter) done by software code running on the PS.
- Observe CPU utilization going up to 100% for one of the two CPUs (this can be seen in the CPU usage graph). In this mode, the frame rate of the video also drops to about 10 fps.

Sobel – HW

- Video processing (edge-detection filtering) done by PL.
- Observe CPU utilization going down (to approximately 0) and the frame rate jumping to 60 fps.

Figure 3-6 shows the detected image edges of the video generated by the TPG, that is, case 1 versus case 2 or 3 of Table 3-1.

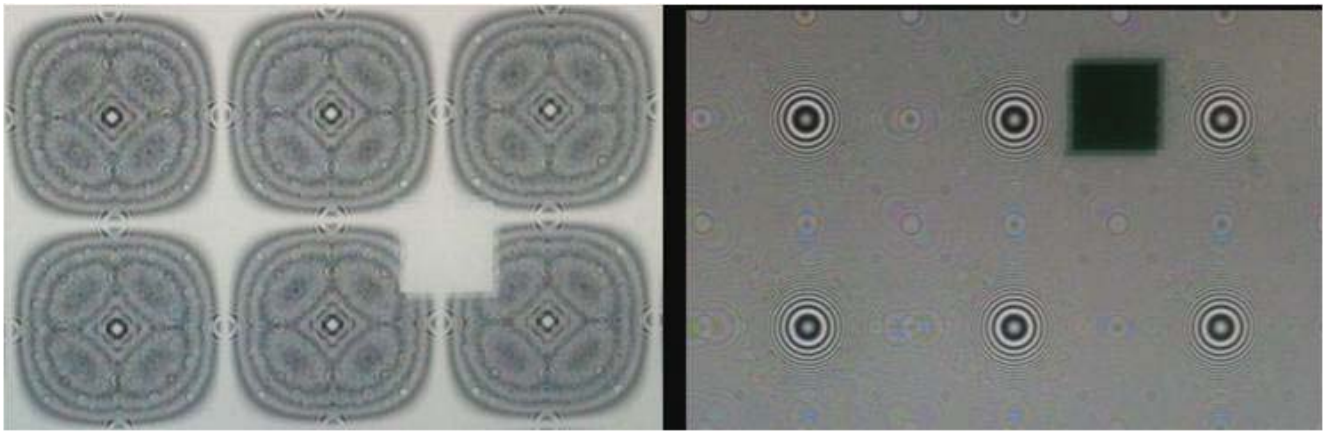

Figure 3-6: **Images with Sobel Filter On (Left) and with Sobel Filter Off (Right)**

While exercising the modes described above, one can observe AXI bus bandwidth utilization and CPU utilization on the graphs in the Qt GUI application.

8. Click **Exit** to quit the application and return the user to Linux console.
9. The application can be restarted by typing the following at the Linux command prompt:

```
zynq> cd /mnt
```

```
zynq> ./run_sobel.sh –qt
```

Running the UART Menu-Based Demonstration Application

A command line based Linux application demonstration is also provided with the package. This application presents the user with a command line menu-based UI to exercise different modes of the video demonstration.

To run the menu-based UI application demonstration, the Qt-based GUI application which was started (as explained in Running the Qt-Based GUI Application Demonstration, page 26) needs to be quit as per step 8, page 29.

The following steps explain how to start the UART menu-based application demonstration and exercise different application video use cases.

10. Go to the UART terminal started on your host PC as explained in step 2 from Running the Qt-Based GUI Application Demonstration, page 26.
11. Type these commands at the Linux command prompt into the host PC based terminal:

```
zynq> cd /mnt
```

```
zynq> ./run_sobel.sh –cmd
```

The menu-based video application demonstration starts as shown in Figure 3-7.

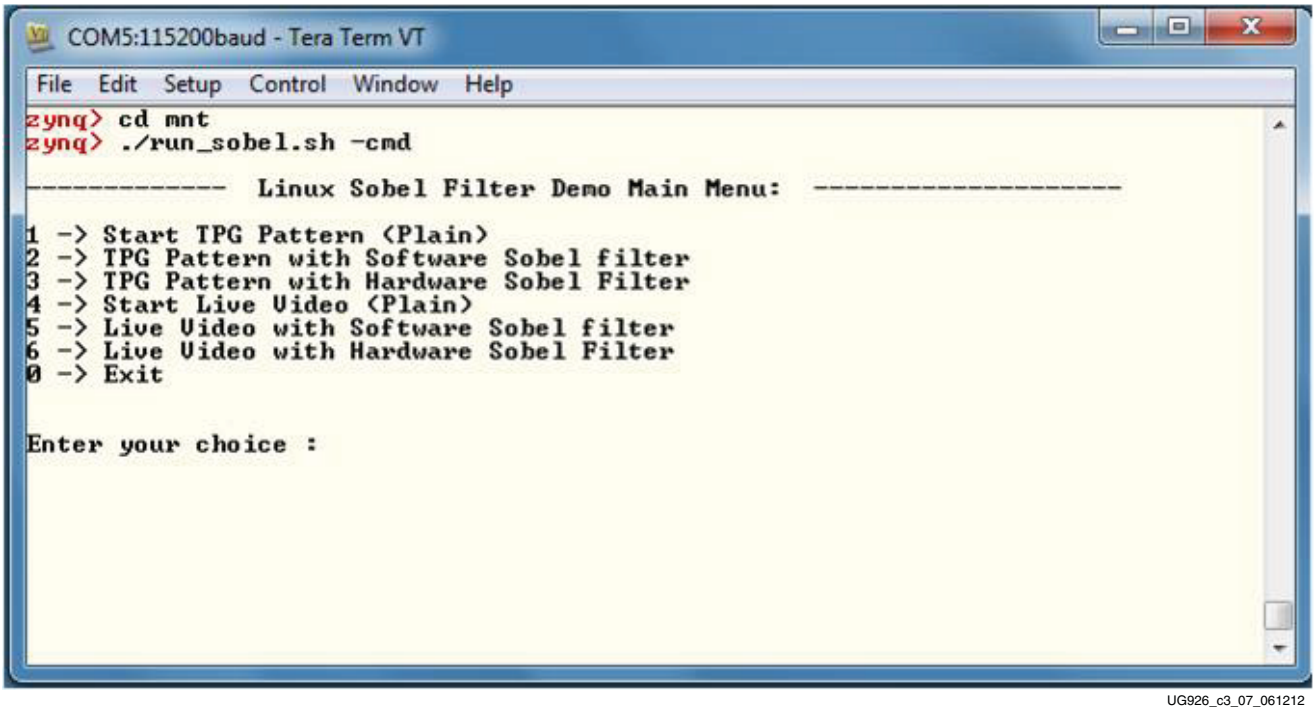

Figure 3-7: **Command Line Based UI Menu**

Exercise different options by entering the use case number displayed in Table 3-2 against `Enter your choice` on the terminal.

Table 3-2: **Zynq-7000 All Programmable SoC Base TRD Video Demonstration Use Cases**

Choice	TPG Control	Sobel Filter Control
1	TPG Pattern	Sobel OFF
2	TPG Pattern	Sobel – SW
3	TPG Pattern	Sobel – HW

Sobel Filter Modes are explained below:

Sobel OFF

- No processing done. Sobel filter is bypassed.

Sobel – SW

- Video processing (edge-detection filter) done by software code running on PS

Sobel On – HW

- Video processing (edge-detection filter) done by PL

  Figure 3-6 shows the detected image edges of the video generated by the TPG, that is, case 1 versus case 2 or 3 of Table 3-2.

12. Enter **0** to exit the application and return to the command prompt.

Evaluating the AMS101 Evaluation Card

Introduction

Each Xilinx Zynq-7000 All Programmable SoC features a 1 MSPS, 12-bit, analog-to-digital converter (ADC) built into the device for everything from simple analog monitoring to more signal processing-intensive tasks like linearization, calibration, over-sampling, and filtering. The ZC702 Evaluation kit includes the hardware and software to evaluate this ADC feature and to determine its usefulness in the user's end system.

For evaluation of Xilinx Agile Mixed Signal (AMS) capability, the following items in the kit are needed:

- Access to the ZC702 XADC header
- AMS101 evaluation card (see Figure 4-1)
- Design and software files, included on the USB key or downloaded from the web
- FPGA design programming files
- USB-UART drivers from Silicon Labs
- Blank SD-MMC card

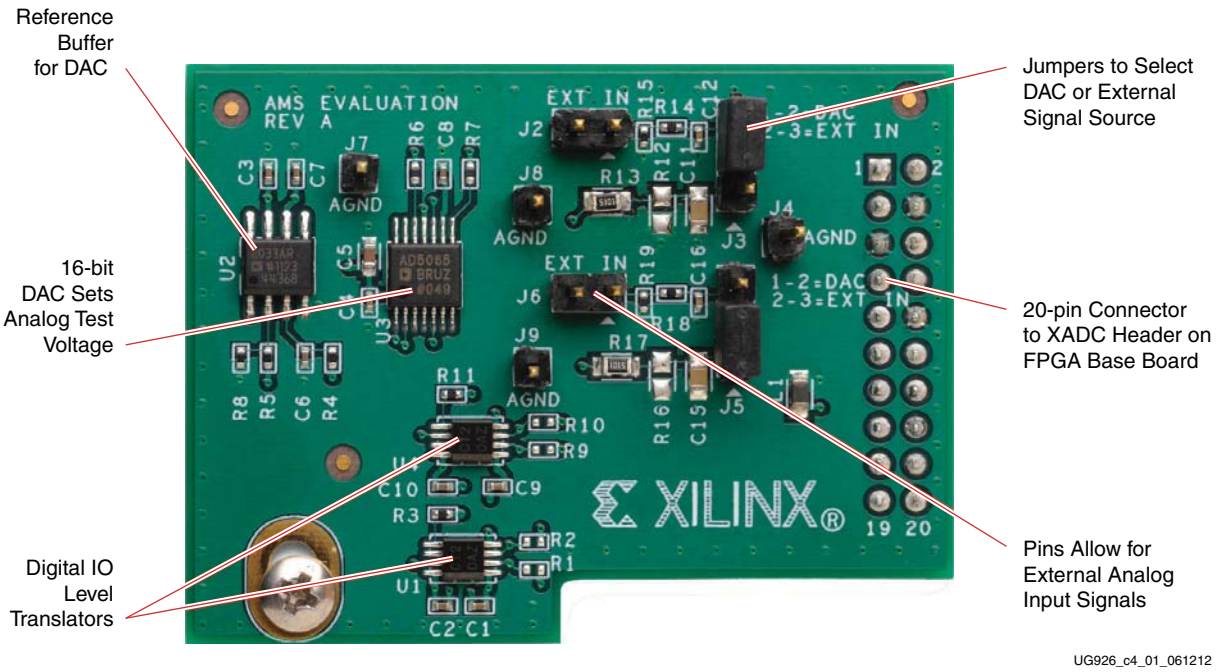

Figure 4-1: **AMS101 Evaluation Card**

Requirements to Get Started

1. The AMS101 evaluation requires a Windows host PC to install the National Instruments LabVIEW Run-Time engine.
2. Verify the USB/UART Silicon Labs drivers are installed as described in Install the USB-UART Driver, page 15.
3. Depending on the computer operating system, select and install one of these National Instruments LabVIEW 2011 Run-Time Engine AMS101 Installers for a 32-bit OS or a 64-bit OS:
   a. LabVIEW 32-bit Run-Time Engine: http://joule.ni.com/nidu/cds/view/p/id/2534/lang/en
   b. LabVIEW 64-bit Run-Time Engine http://joule.ni.com/nidu/cds/view/p/id/2536/lang/en
4. Unzip the `AMS_Eval_Demo_Files_<ISE_Version>` from the `ZC702_Reference_Designs` folder on the USB stick to access the AMS bitstream (`boot.bin`).
5. Copy the `boot.bin` file on an SD-MMC card.

Evaluating AMS

1. Connect and power the hardware.
   a. Connect the ZC702 board to the AMS101 evaluation card, making sure the notch on the XADC header lines up correctly with the AMS101 evaluation card. See Figure 4-2.

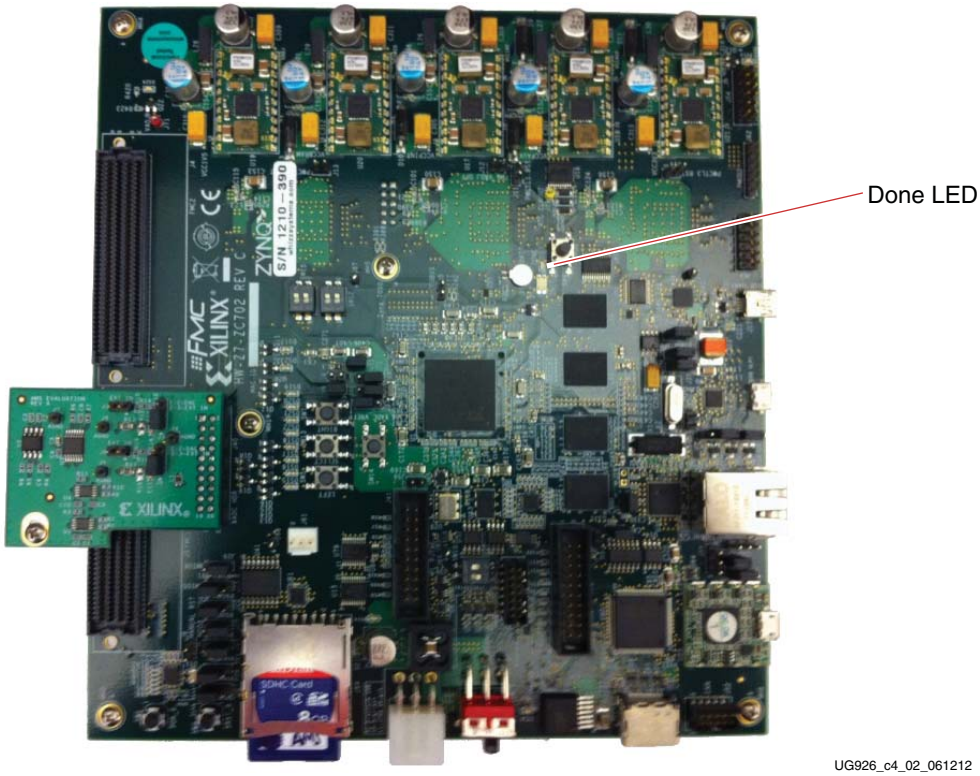

Figure 4-2: **ZC702 Board with AMS101 Evaluation Card Plugged into XADC Header**

2. Download the design to the Zynq-7000 All Programmable SoC.
   a. Open `AMS101 Evaluator GUI V1.0.exe` from the directory and `AMS_Eval_Demo_Files_<ISE_Version>` from the location it was copied to, from the USB stick.
   b. Copy the `boot.bin` file on the SD-MMC card.
   c. Plug the SD-MMC card into the ZC702 board.
   d. Set the ZC702 board switch settings to *boot from SD* mode (see Figure 3-3).
   e. Power on the ZC702 board. After about 15 seconds, the Done LED (DS3) turns green, indicating the design file on the SD-MMC card has properly loaded onto the Zynq-7000 All Programmable SoC.
3. Run the AMS101 Evaluator LabVIEW GUI executable file.

a. On the Host PC, open `AMS101 Evaluator GUI V1.0.exe` from the directory and `AMS_Eval_Demo_Files_<ISE_Version>` from the location it was copied to, from the USB stick.

The AMS Evaluator Tool allows designers to quickly evaluate the analog signals in the time and frequency domain, display linearity, verify the XADC register settings, and measure the internal temperature sensor and supply voltages.

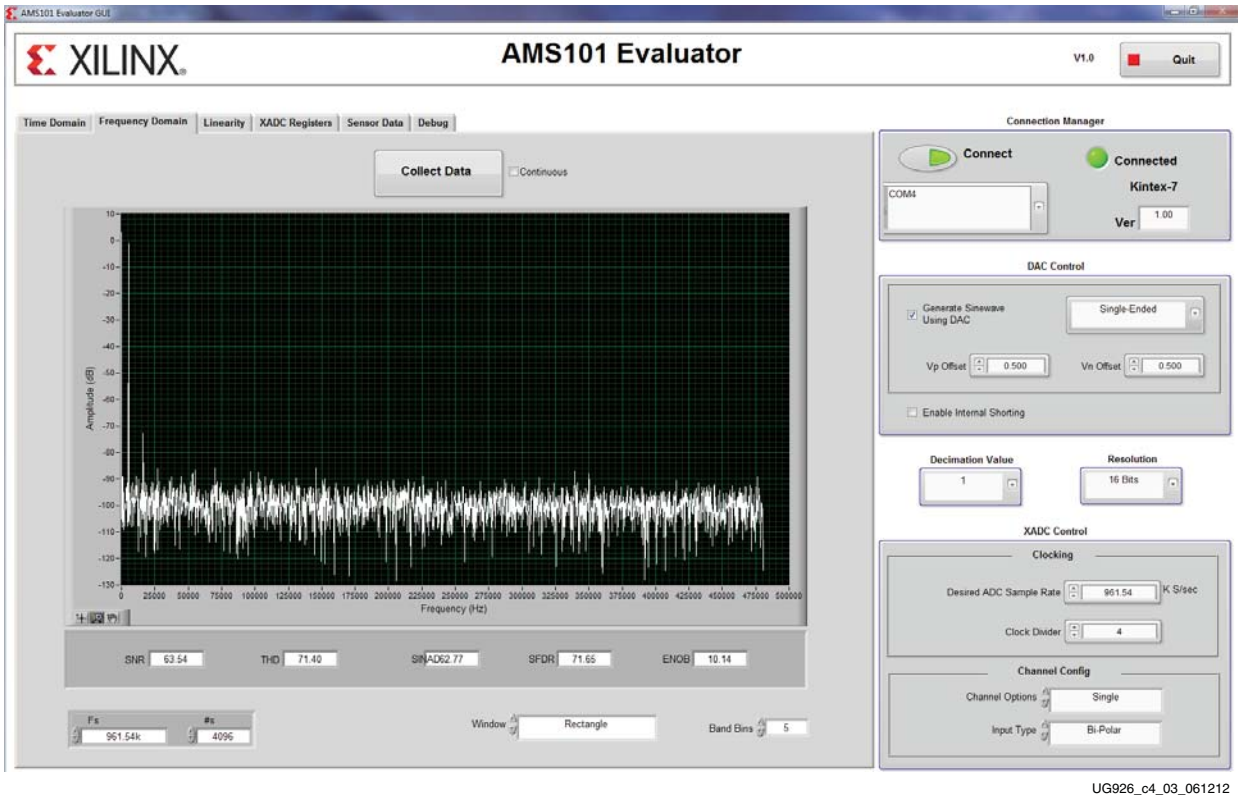

Figure 4-3: **AMS101 Evaluator GUI**

AMS Evaluator GUI source code is not provided.

For a more extensive explanation of the AMS101 evaluation card and the applicable files on the USB key, refer to UG886, *AMS101 Evaluation Card User Guide* [Ref 9].

Next Steps

For more information on reference designs included in this kit, software, and additional tutorials, including how to restore the default content of the onboard nonvolatile storage, see the ZC702 board resource page [Ref 3].

Appendix A

Additional Resources

Xilinx Resources

To search the Answer database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx Support website at www.xilinx.com/support

For a glossary of technical terms used in Xilinx documentation, see http://www.xilinx.com/company/terms.htm

To find additional documentation, see the Xilinx website at http://www.xilinx.com/support/documentation/index.htm

References

These documents provide supplemental material useful with this guide:

1. Zynq-7000 All Programmable SoC product table http://www.xilinx.com/publications/prod_mktg/zynq7000/Zynq-7000-combined-product-table.pdf
2. Zynq-7000 All Programmable SoC platform page http://www.xilinx.com/products/silicon-devices/epp/zynq-7000
3. Xilinx Zynq-7000 SoC ZC702 Evaluation Kit product page http://www.xilinx.com/ZC702
4. UG873, *Zynq-7000 Concepts, Tools, and Techniques Guide*
5. Zynq-7000 documentation page http://www.xilinx.com/support/documentation/zynq-7000.htm
6. UG850, *ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide*
7. UG925, *Zynq-7000 All Programmable SoC ZC702 Base Targeted Reference Design User Guide*

8. Silicon Labs USB-UART drivers
   http://www.silabs.com/Support%20Documents/Software/CP210x_VCP_Win_XP_S2K3_Vista_7.exe
9. UG886, *AMS101 Evaluation Card User Guide*

Additional Useful Sites for Boards and Kits

More information on the Zynq-7000 All Programmable SoC family boards, FMC extension cards, and other kits based on Zynq-7000 architecture is available at this website:

10. Xilinx Zynq-7000 SoC Boards and Kits
    http://www.xilinx.com/products/boards_kits/zynq-7000.htm

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