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## NC7SZ34 TinyLogic® UHS Buffer

### Features

- Ultra-High Speed:  $t_{PD}$  2.4ns (Typical) into 50pF at 5V  $V_{CC}$
- High Output Drive:  $\pm 24mA$  at 3V  $V_{CC}$
- Broad  $V_{CC}$  Operating Range: 1.65V to 5.5V
- Matches Performance of LCX Operated at 3.3V  $V_{CC}$
- Power-Down High-Impedance Inputs / Outputs
- Proprietary Noise / EMI Reduction Circuitry
- WLCSP Package

### Description

The NC7SZ34 is a single buffer from Fairchild's Ultra-High Speed (UHS) series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive, while maintaining low static power dissipation over a broad  $V_{CC}$  operating range of 1.65V to 5.5V  $V_{CC}$ . The inputs and output are high-impedance when  $V_{CC}$  is 0V. Inputs tolerate voltages up to 7V, independent of  $V_{CC}$  operating voltage.

### Related Resources

- [AN-5055 — Portability and Ultra Low Power TinyLogic®](#)
- [MS-503 — Family Characteristics TinyLogic® HS/HST and UHS Series](#)

### Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SZ34UCX	KJ	4-Lead, Wafer-Level Chip Scale 0.76x0.76x0.5mm Wafer-Level Chip-Scale Package (WLCSP)	3000 Units on Tape & Reel

## Pin Configurations

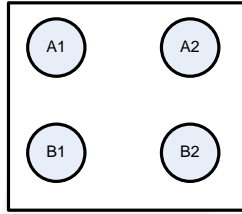


Figure 1. WLCSP (Top View)

## Pin Definitions

WLCSP	Name	Description
A1	A	Input
A2	VCC	Power Supply
B1	GND	Ground
B2	Y	Output

## Function Table

Y = A

Inputs	Output
<b>A</b>	<b>Y</b>
LOW Logic Level	LOW Logic Level
HIGH Logic Level	HIGH Logic Level

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
$V_{CC}$	Supply Voltage		-0.5	7.0	V
$V_{IN}$	DC Input Voltage		-0.5	7.0	V
$V_{OUT}$	DC Output Voltage		-0.5	7.0	V
$I_{IK}$	DC Input Diode Current	$V_{IN} < -0.5V$		-50	mA
$I_{OK}$	DC Output Diode Current	$V_{OUT} < -0.5V$		-50	mA
$I_{OUT}$	DC Output Current			±50	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current			±50	mA
$T_{STG}$	Storage Temperature Range		-65	+150	°C
$T_J$	Junction Temperature Under Bias			+150	°C
$T_L$	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
$P_D$	Power Dissipation at +85°C			200	mW
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charge Device Model, JEDEC:JESD22-C101			2000	

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{CC}$	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.5	5.5	
$V_{IN}$	Input Voltage		0	5.5	V
$V_{OUT}$	Output Voltage		0	$V_{CC}$	V
$T_A$	Operating Temperature		-40	+85	°C
$t_r, t_f$	Input Rise and Fall Times	$V_{CC}$ at 1.8V, 2.5V ±0.2V	0	20	ns/V
		$V_{CC}$ at 3.3V ±0.3V	0	10	
		$V_{CC}$ at 5.0V ±0.5V	0	5	
$\theta_{JA}$	Thermal Resistance			80	°C/W

### Note:

- Unused inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> =25°C			T <sub>A</sub> =-40 to 85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	1.65 to 1.95		0.65V <sub>CC</sub>			0.65V <sub>CC</sub>		V
		2.30 to 5.50		0.70V <sub>CC</sub>			0.70V <sub>CC</sub>		
V <sub>IL</sub>	LOW Level Input Voltage	1.65 to 1.95				0.35V <sub>CC</sub>		0.35V <sub>CC</sub>	V
		2.30 to 5.50				0.30V <sub>CC</sub>		0.30V <sub>CC</sub>	
V <sub>OH</sub>	HIGH Level Output Voltage	1.65	V <sub>IN</sub> =V <sub>IH</sub> , I <sub>OH</sub> =-100μA	1.55	1.65				V
		1.80		1.70	1.80		1.70		
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I <sub>OH</sub> =-4mA	1.29	1.52		1.29		
		2.30	I <sub>OH</sub> =-8mA	1.90	2.15		1.90		
		3.00	I <sub>OH</sub> =-16mA	2.40	2.80		2.40		
		3.00	I <sub>OH</sub> =-24mA	2.30	2.68		2.30		
		4.50	I <sub>OH</sub> =-32mA	3.80	4.20		3.80		
V <sub>OL</sub>	LOW Level Output Voltage	1.65	V <sub>IN</sub> =V <sub>IL</sub> , I <sub>OL</sub> =100μA		0.00	0.10		0.10	V
		1.80			0.00	0.10		0.10	
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65	I <sub>OL</sub> =4mA		0.08	0.24		0.24	
		2.30	I <sub>OL</sub> =8mA		0.10	0.30		0.30	
		3.00	I <sub>OL</sub> =16mA		0.15	0.40		0.40	
		3.00	I <sub>OL</sub> =24mA		0.22	0.55		0.55	
		4.50	I <sub>OL</sub> =32mA		0.22	0.55		0.55	
I <sub>IN</sub>	Input Leakage Current	0 to 5.5	0 ≤ V <sub>IN</sub> ≤ 5.5V			±1		±10	μA
I <sub>OFF</sub>	Power Off Leakage Current	0	V <sub>IN</sub> or V <sub>OUT</sub> =5.5V			1		10	μA
I <sub>CC</sub>	Quiescent Supply Current	1.65 to 5.50	V <sub>IN</sub> =5.5V, GND			1.0		10	μA

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	T <sub>A</sub> =25°C			T <sub>A</sub> =-40 to 85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay	1.65	C <sub>L</sub> =15pF, R <sub>L</sub> =1MΩ	2.0	5.3	11.4	2.0	12.0	ns	Figure 2 Figure 3
		1.80		2.0	4.4	9.5	2.0	10.0		
		2.5 ±0.2		0.8	2.9	6.5	0.8	7.0		
		3.3 ±0.3		0.5	2.1	4.5	0.5	4.7		
		5.0 ±0.5		0.5	1.8	3.9	0.5	4.1		
		3.3 ±0.3		C <sub>L</sub> =50pF, R <sub>L</sub> =500Ω	1.5	2.9	5.0	1.5		
		5.0 ±0.5	0.8		2.4	4.3	0.8	4.5		
C <sub>IN</sub>	Input Capacitance	0.00			2.0				pF	
C <sub>PD</sub>	Power Dissipation Capacitance <sup>(2)</sup>	3.30			12.9				pF	Figure 4
		5.00			15.6					

**Note:**

- C<sub>PD</sub> is defined as the value of the internal equivalent capacitance derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output lading and operating at 50% duty cycle. C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression: I<sub>CCD</sub>=(C<sub>PD</sub>)(V<sub>CC</sub>)(f<sub>IN</sub>)+(I<sub>CC</sub>Static).

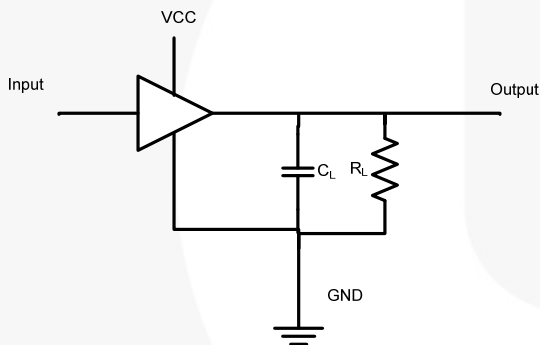


Figure 2. AC Test Circuit

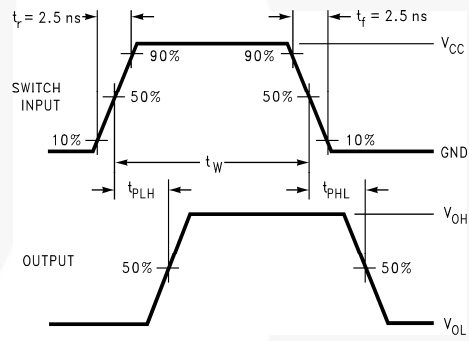


Figure 3. AC Waveforms

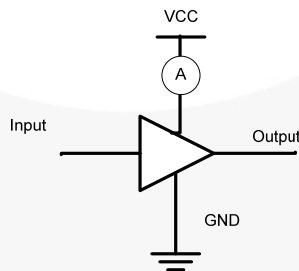
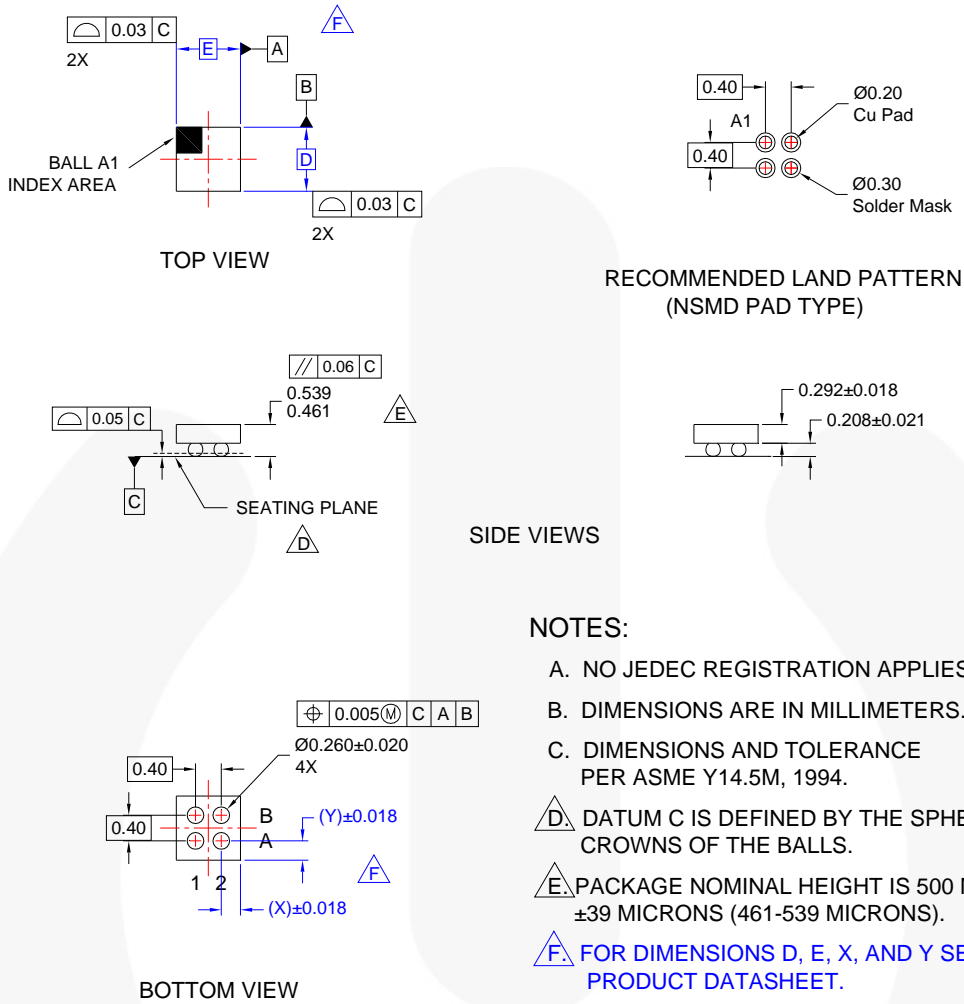


Figure 4. I<sub>CCD</sub> Test Circuit

**Note:**

- Input=AC Waveform; t<sub>r</sub>=t<sub>f</sub>=1.8ns; Frequency =10MHz; Duty Cycle =50%.

## Physical Dimensions



**Figure 5. 4-Lead, Wafer-Level Chip Scale 0.76x0.76x0.5mm Wafer-Level Chip-Scale Package (WLCSP)**

Product	D	E	X	Y
NC7SZ34UCX	0.76 +/-0.030	0.76 +/-0.030	0.18	0.18

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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
UCX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
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