0.7A, 36V, 2.1MHz Synchronous Small Form Factor Step-Down Converter

General Description

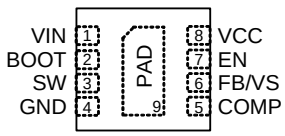
The RTQ2130B is a high-efficiency, monolithic synchronous step-down DC-DC converter that can deliver up to 0.7A output current from a 3V to 36V widely input supply. The RTQ2130B current-mode control with external compensation allows the transient response to be optimized over various loads and output capacitors. Cycle-by-cycle current limit provides protection against short-circuit output, and soft-start can eliminate input current surge during startup. Input under-voltage lockout, output under-voltage protection, over-current protection and over-temperature protection offer completely safe and smooth operation in all applied conditions. The RTQ2130B is fully specified over the temperature range of T_A = –40°C to 125°C and is available in WDFN-8SL 2x3 package.

Applications

- Automotive Systems
- Car Camera Module and Car Cockpit Systems
- Connected Car Systems
- Point of Load Regulator in Distributed Power Systems
- Digital Set Top Boxes
- Broadband Communications

Pin Configuration

(TOP VIEW)



WDFN-8SL 2x3

Features

- **AEC-Q100 Grade 1 Qualified**
- **Wide Input Voltage Range**
  - **4V to 36V**
  - **3V to 36V (Soft-start is finished)**
- **99% Duty Cycle Operation**
- **Tight Switching Frequency Variation 2.1MHz ± 10% Over Operating Ambient Temperature**
- **5V Fixed Output Voltage (see Ordering Information for availability)**
- **0.7A Output Current**
- **–40°C to 125°C Operating Ambient Temperature Range**
- **Current-Mode Control**
- **Integrated 200mΩ/160mΩ MOSFETs**
- **Enable Control**
- **Over-Temperature Protection**
- **Output Under-Voltage Protection with Hiccup Mode**
- **Adjacent Pin Short-Circuit Protection**
- **Cycle-by-Cycle Over-Current Protection**
- **Input Under-Voltage Lockout**
- **RoHS Compliant and Halogen Free**

Ordering Information

RTQ2130B (-□□) □□-QT

Grade
QT : AEC-Q100 Qualified

Package Type
QW : WDFN-8SL 2x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Fixed Output Voltage
50 : 5V

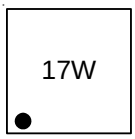
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

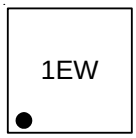
RTQ2130BGQW-QT



17 : Product Code

W : Date Code

RTQ2130B-50GQW-QT



1E : Product Code

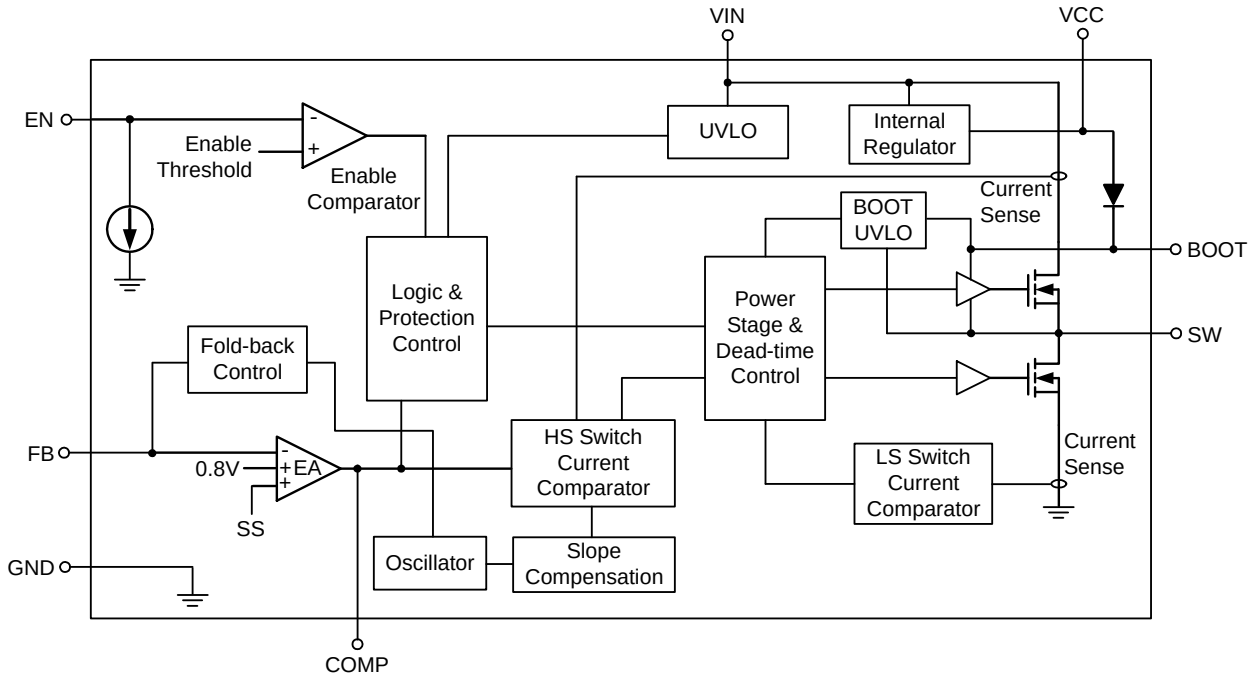
W : Date Code

Functional Pin Description

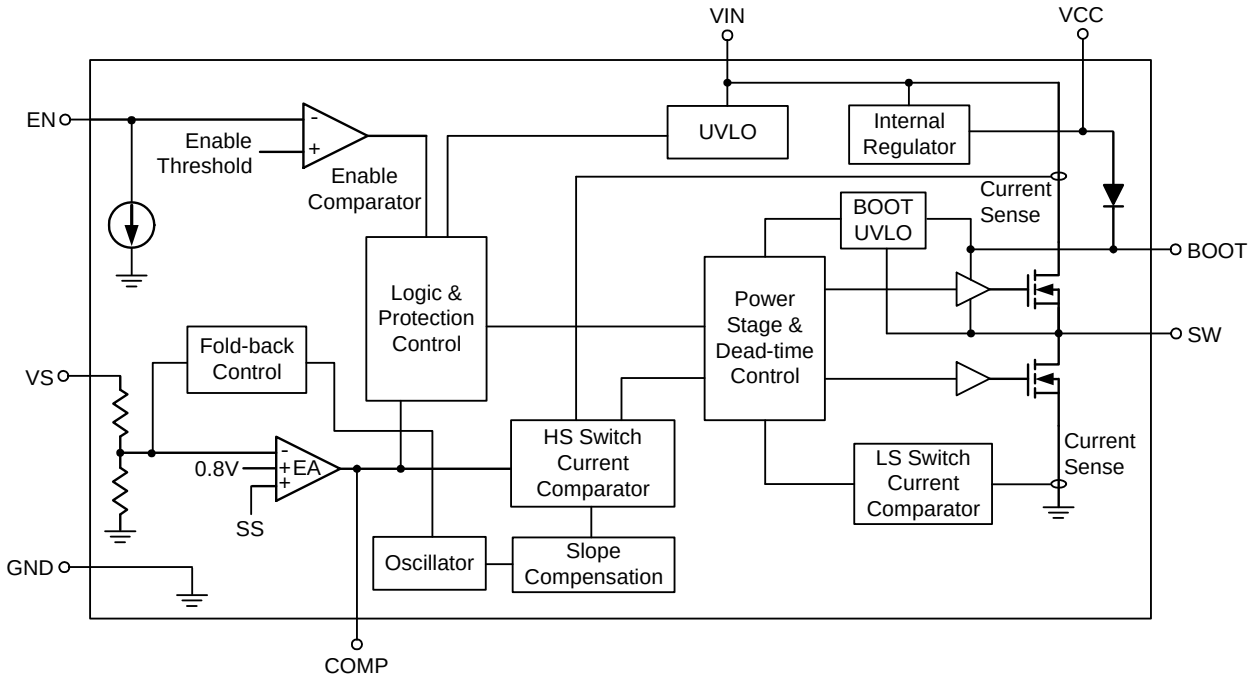
Pin No.	Pin Name	Pin Function
1	VIN	Supply input. Supply the power to the internal control circuit as well as the power switches of the device. Drive VIN with a 3V to 36V power source and bypass VIN to GND with a suitable large capacitor to eliminate noise.
2	BOOT	Bootstrap supply for high-side gate driver. Connect a 100nF or greater capacitor from SW to BOOT to power the high-side switch.
3	SW	Switch node. SW is the switching node that supplies power to the output and connect the output LC filter from SW to the output load.
4	GND	System ground. Provide the ground return path for the control circuitry and low-side power MOSFET.
5	COMP	Compensation node. The current comparator threshold increases with this control voltage. Connect external compensation elements to this pin to stabilize the control loop.
6	FB/VS	Output voltage sense. There are two output voltage setting options : one is a fixed output voltage available for the VS pin, and the other is through a resistive divider to sense the output voltage at the FB pin. The feedback reference voltage is 0.8V typically.
7	EN	Enable control input. Connect this pin to logic high can enable the device and connect this pin to GND can disable the device.
8	VCC	Linear regulator output. VCC is the output of the internal 5V linear regulator powered by VIN. Decouple with a 1μF ceramic capacitor from VCC to ground for normal operation.
9 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PCB copper area for maximum power dissipation.

Functional Block Diagram

Adjustable Output Voltage



Fixed 5V Output Voltage



Operation

Switching Frequency and Operational Duty Cycle

With normal duty cycle, the RTQ2130B operates at fixed switching frequency = 2.1MHz. If the duty cycle is too high/low, in order to extend the operational input voltage range, the RTQ2130B is forced to lower its switching frequency by skipping on/off pulses.

The minimum on time of the RTQ2130B is 60ns (typ., at I_{OUT} = 0.5A). If input voltage is too high and the required on pulse width becomes smaller than minimum on time, IC starts to skip on pulse once the $V_{(COMP)}$ has reached its low clamped value.

The minimum off time of the RTQ2130B is 60ns (typ.). If input voltage drops and the required off pulse width becomes smaller than minimum off time, IC starts to skip off pulse and keeps H/S MOSFET on continuously. With this feature, IC can support > 99% duty cycle.

Input Under-Voltage Lockout Threshold

The RTQ2130B includes an input under-voltage lockout protection (UVLO) circuit. If input voltage exceeds a UVLO rising threshold voltage (V_{UVLO}), the converter will reset and prepare the PWM for operation. If the input voltage falls below a UVLO falling threshold voltage (i.e. $V_{UVLO} - \Delta V_{UVLO}$) during normal operation, the converter will stop switching. There is some hysteresis between UVLO rising and falling threshold voltages to prevent a reset caused by noise.

Note that V_{IN} = 3V is only design for cold crank requirement. Normal input voltage should be larger than UVLO rising threshold to turn on.

Chip Enable

The EN pin is the chip enable input. Pulling the EN pin low to 1.25V (typ) will disable output voltage and low to 0.4V will shut down the device. During shutdown mode, the shutdown current of the RTQ2130B is lower than 10μA. The EN pin has an internal pull-down current source. When VCC exceeds 5V, the current source typically sinks 1.2μA for V_EN < 4V and up to 70μA for V_EN > 4V.

Internal Regulator

The internal regulator generates a 5V regulated voltage, V_{CC}, to drive internal circuit. When V_{IN} is below 5V, V_{CC} will track with VIN. A capacitor (= 1μF), connected from VCC to GND, is required.

Internal Soft-Start Function

The RTQ2130B provides an internal soft-start function. The soft-start function is used to prevent large inrush current while the converter is being powered-up. The typical soft-start time (i.e. for the FB voltage to ramp from 0V to 0.8V) is 2ms.

When voltage of EN pin exceeds threshold voltage, VCC will start up first and after 0.8ms output voltage ramp up during soft-start time as shown in Figure 1.

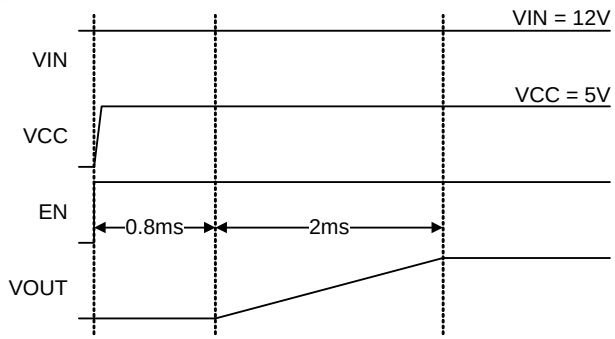


Figure 1. Soft-Start Sequence

High-Side MOSFET Over-Current Limit

IC detects the inductor current during the period high-side MOSFET turns on. When inductor current reaches the current limit value, IC will turn off high-side MOSFET, so it can provide cycle-by-cycle peak current limit protection to prevent IC from over current.

Low-Side MOSFET Over-Current Limit

The RTQ2130B not only implements the high-side switch current limit but also provides the low-side switch sourcing current limit and low-side switch sinking current limit for low-side MOSFET. With these current protections, the IC can easily control inductor current at both side power switches and avoid current runaway for short-circuit condition.

For the low-side switch sourcing current limit, there is a specific comparator in internal circuitry to compare the low-side MOSFET sourcing current to the internal set current limit at the end of every clock cycle. When the low-side sourcing current is higher than the set sourcing limit, the high-side power switch is not turned on and low-side power switch is kept on until the following clock cycle for releasing the above sourcing current to the load. It is allowed to turn on the high-side MOSFET again when the low-side current is lower than the set sourcing current limit at the beginning of a new cycle.

For the low-side switch sinking current limit protection, it is implemented by detecting the voltage across the low-side power switch. If the low-side reverse current exceeds the set sinking limit, both power switches are off immediately, and it is held to stop switching until the beginning of next cycle.

Output Under-Voltage Protection

The RTQ2130B includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold, 50% (typ.) of the internal reference voltage, the UV comparator will go high to turn off the internal high-side MOSFET switches. If the output under-voltage condition continues for a period of time, the RTQ2130B will enter output under-voltage protection with hiccup mode. During hiccup mode, the device remains shut down. After a period of time, a soft-start sequence for auto-recovery will be initiated. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed. The UVP profile is shown in Figure 2.

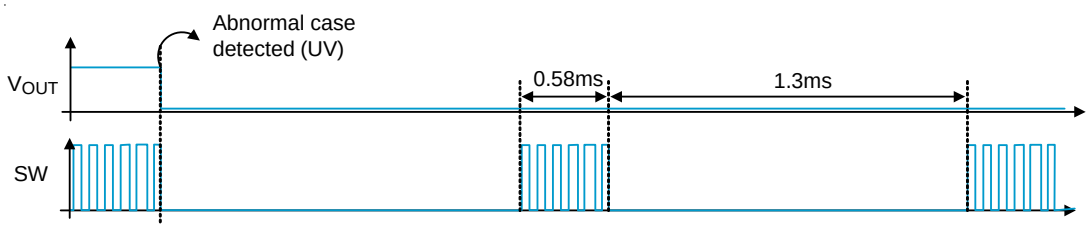


Figure 2. Output Under-Voltage Protection with Hiccup Mode

Over-Temperature Protection

Over-temperature protection is implemented to prevent the chip from operating at excessively high temperatures. When the junction temperature is higher than 175°C, the OTP will shut down switching operation. The chip will automatically resume normal operation with a complete soft-start sequence once the junction temperature cools down by approximately 15°C.

Adjacent Pin Short-Circuit Protection

The RTQ2130B provide adjacent Pin short-circuit protection.

For the RTQ2130B, an internal protection fuse will be blown to prevent IC smoke, fire and spark when the BOOT pin is shorted to VIN pin.

Hiccup mode protection will be triggered to prevent the IC from being burned out when the SW pin is shorted to GND.

BOOT UVLO

To ensure that high-side switch can be controlled normally, the RTQ2130B implements BOOT UVLO function to prevent operation under low $V_{(BOOT-SW)}$ condition. When $V_{(BOOT-SW)}$ is lower than BOOT_UVLO_L level 2.5V (typ.), IC will disable 99% duty cycle operation, and the minimum off time will be enlarged to 100ns (typ.) to extend BOOT charging time. BOOT UVLO condition will be removed after $V_{(BOOT-SW)}$ is higher than 2.8V (typ.).

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 42V
- Switch Voltage, SW ---------- –0.3V to 42V
  <100ns ---------- –5V to 46.3V
- BOOT to SW, V_{BOOT} – V_{SW} ---------- –0.3V to 6V
- EN Voltage, EN ---------- –0.3V to 42V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8SL 2x3 ---------- 3.05W
- Package Thermal Resistance (Note 2)
  WDFN-8SL 2x3, θ_{JA} ---------- 41°C/W
  WDFN-8SL 2x3, θ_{JC} ---------- 9.7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage ---------- 3V to 36V
- Output Voltage ---------- 0.8V to 28V
- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Operating Voltage	V_{IN}	Soft-start is finished	3	--	36	V
Under-Voltage Lockout Threshold	V_{UVLO}	VIN rising	3.6	3.8	4	V
Under-Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	900	--	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	10	μA
Quiescent Current	I_Q	V_{EN} = 2V, not switching	--	1.1	1.3	mA
Enable Voltage						
Enable Threshold Voltage	V_{IH}	V_{EN} rising	1.3	1.45	1.6	V
	V_{IL}	V_{EN} falling	1.1	1.25	1.4	
Output Voltage						
Output Voltage Sense (Note5)	V_S	V_S = 5V	4.9	5	5.1	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage	V_{REF}	3V ≤ V_{IN} ≤ 36V	0.788	0.8	0.812	V
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}	V_{BOOT} – V_{SW} = 4.8V, minimum duty cycle	1.02	1.2	1.43	A
Low-Side Switch Sourcing Current Limit	I_{sr_L}	From source to drain	0.935	1.1	1.265	A
Low-Side Switch Sinking Current Limit	I_{sk_L}	From drain to source	--	0.8	--	A
Switching						
Switching Frequency	f_{SW}		1890	2100	2310	kHz
Minimum On-Time	t_{ON_MIN}		--	60	80	ns
Internal MOSFET						
High-Side On-Resistance	$R_{DS(ON)\_H}$		--	200	360	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_L}$		--	160	288	
Soft-Start						
Soft-Start Time	t_{SS}		1.3	2	2.7	ms
Error Amplifier						
Error Amplifier Trans-Conductance	gm	–10μA < I_{COMP} < 10μA	665	950	1235	μA/V
COMP to Current Sense Trans-Conductance	gm_{CS}		0.85	1.2	1.45	A/V
Over-Temperature Protection						
Thermal Shutdown	T_{SD}		--	175	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	15	--	

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

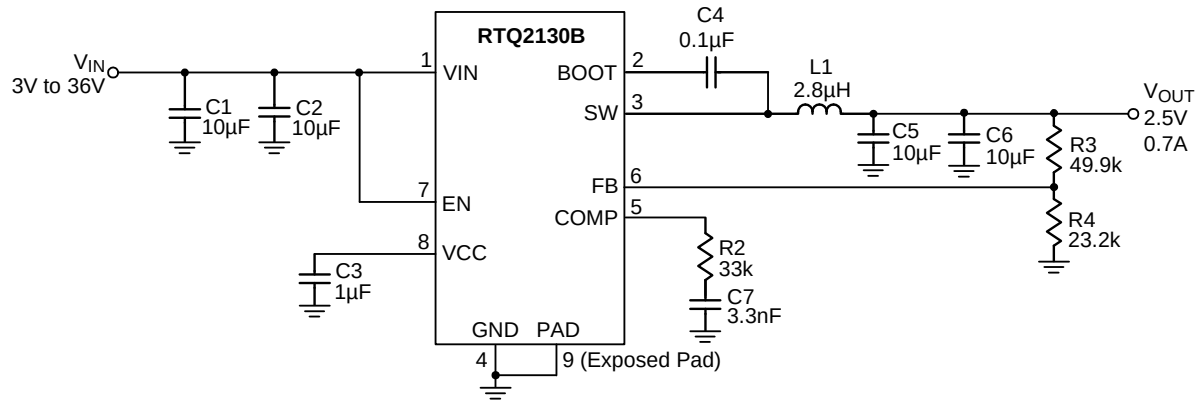
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

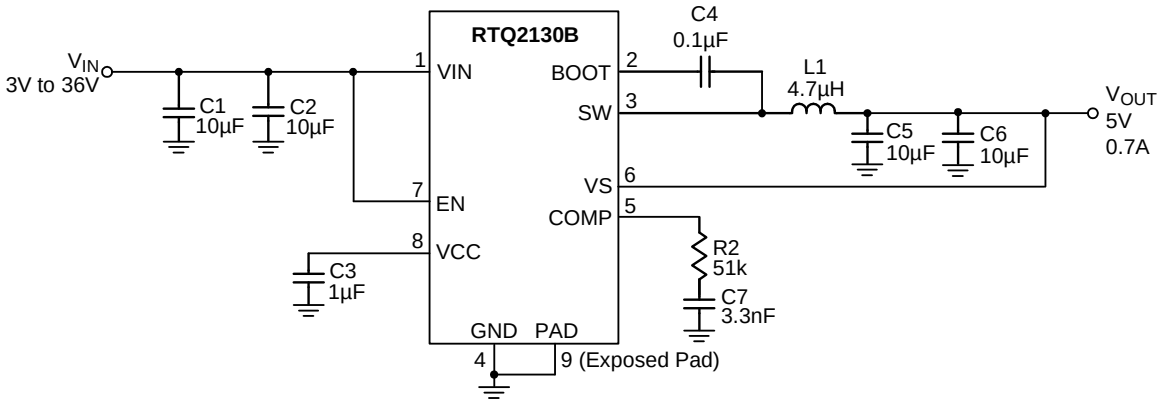
Note 5. There are two output voltage setting options : one is that trimmed output voltage options for a fixed output voltage are available for the VS pin, and the other is through a resistive divider to sense the output voltage at the FB pin.

Typical Application Circuit

Adjustable Output Voltage



Fixed 5V Output Voltage

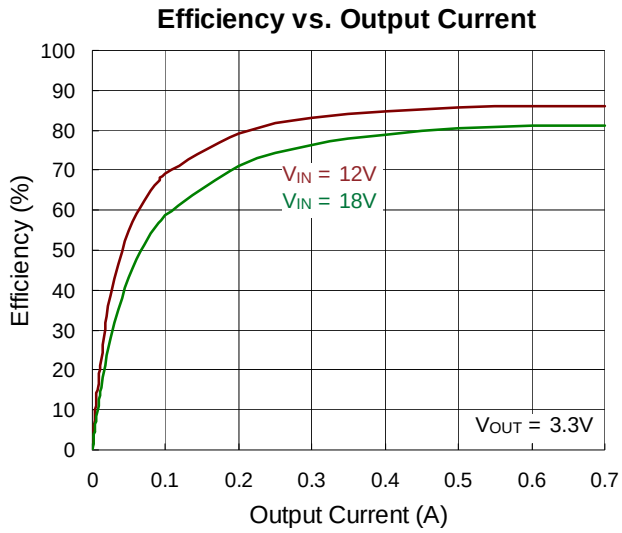


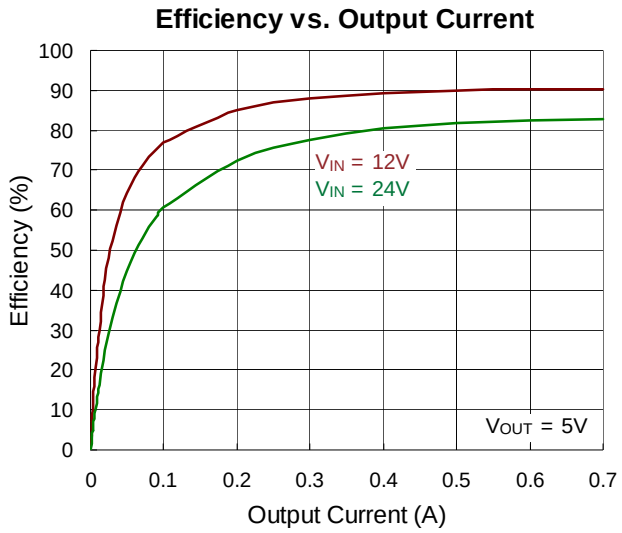
Note : All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

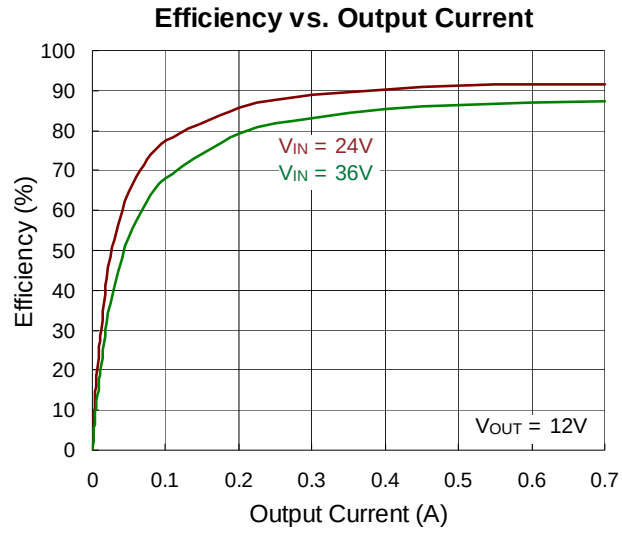
Table 1. Suggested Component Values for Adjustable Output Voltage Version

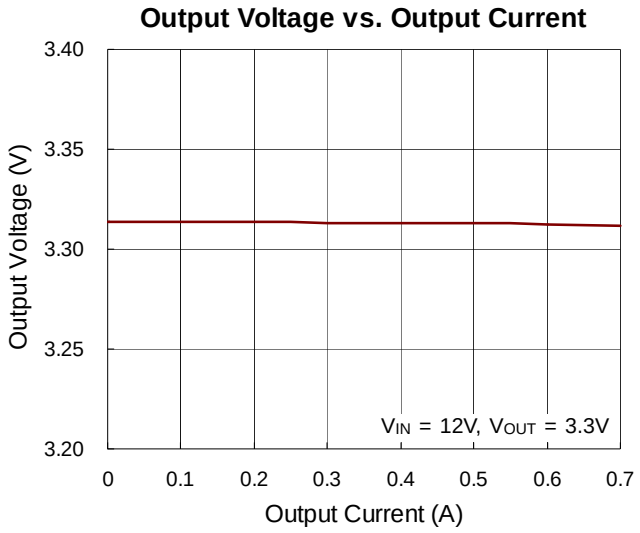
V_{OUT} (V)	R3 (kΩ)	R4 (kΩ)	L1 (µH)	C_{OUT} (µF)	R2 (kΩ)	C7 (nF)
1	4.99	20	2.2	20	10	3.3
1.2	10	20	2.2	20	12	3.3
1.8	30	24	2.2	20	17.4	3.3
2.5	49.9	23.2	2.8	20	33	3.3
3.3	75	24	3.3	20	39	3.3
5	105	20	4.7	20	51	3.3

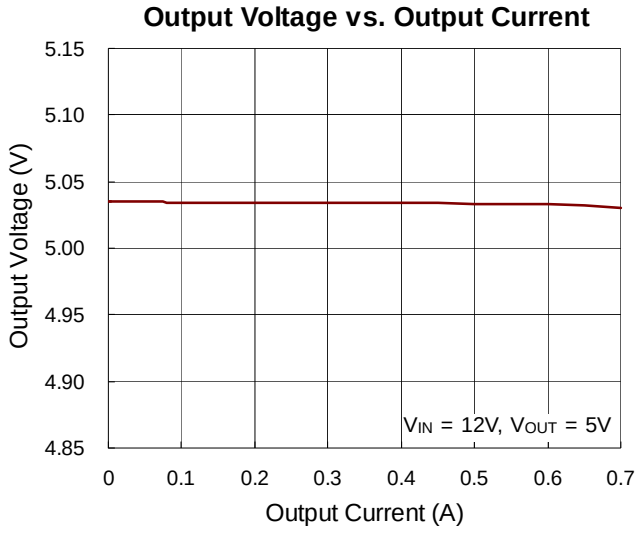
Typical Operating Characteristics

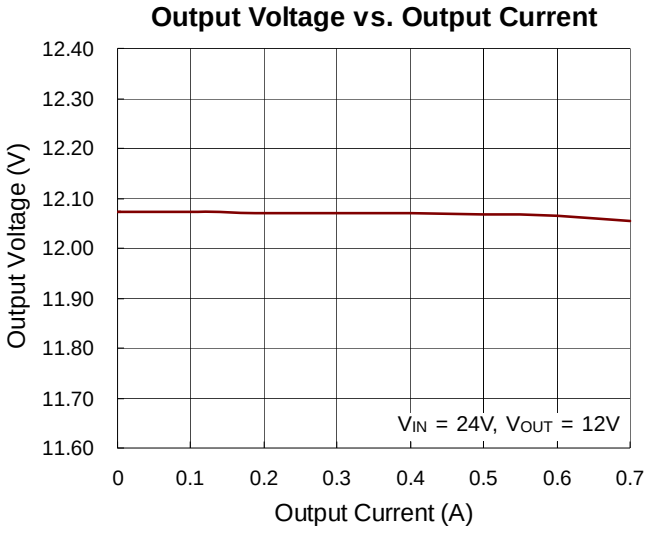




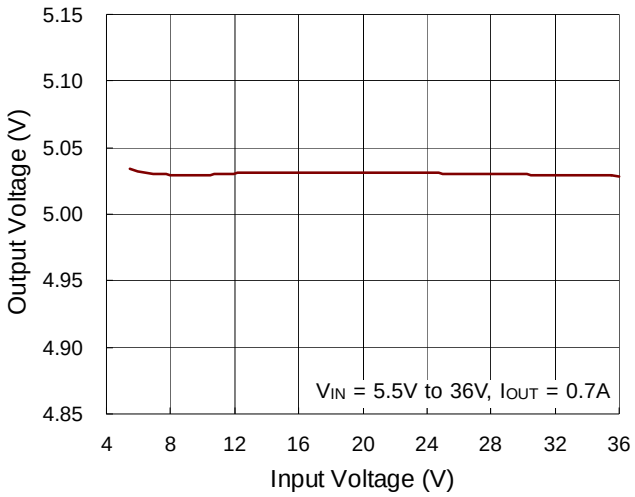




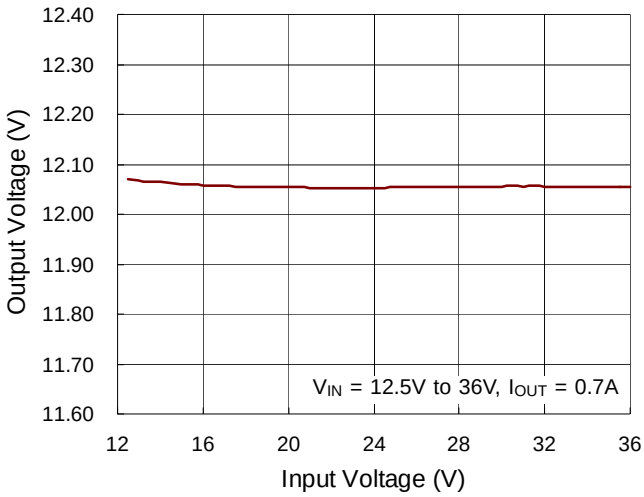




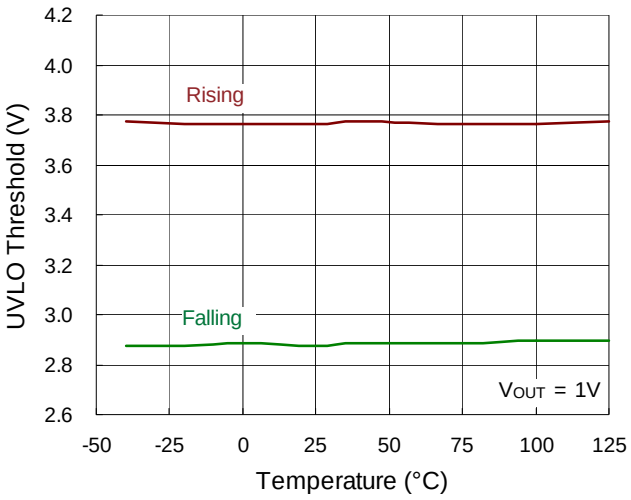
Output Voltage vs. Input Voltage



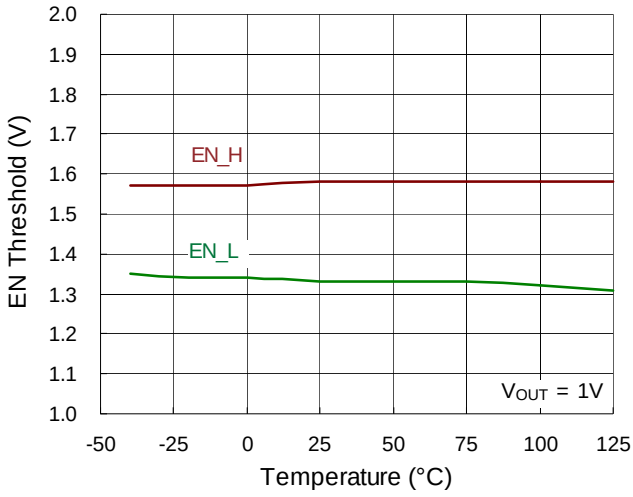
Output Voltage vs. Input Voltage



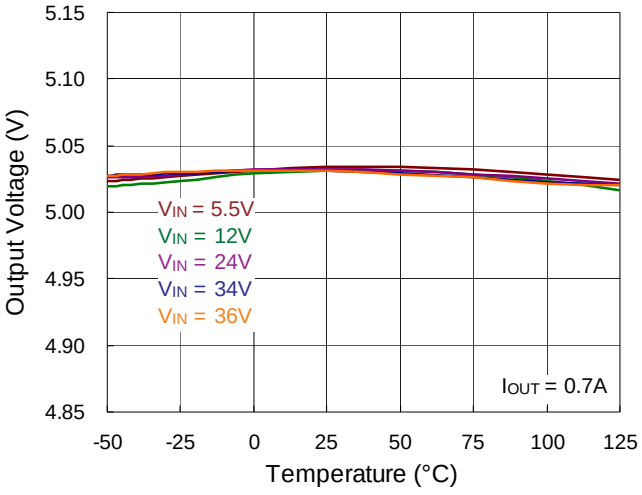
UVLO Threshold vs. Temperature



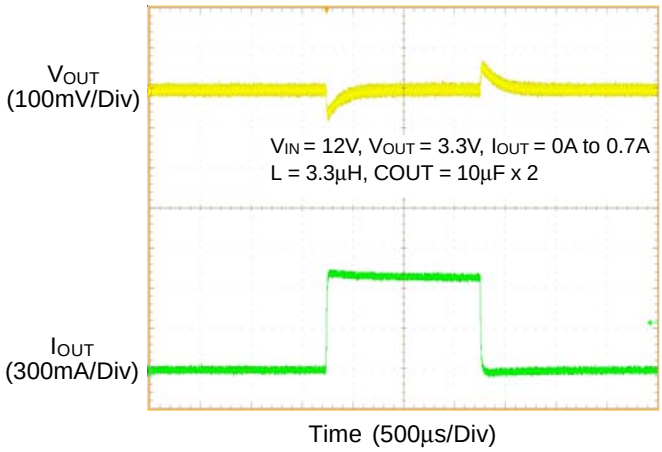
EN Threshold vs. Temperature



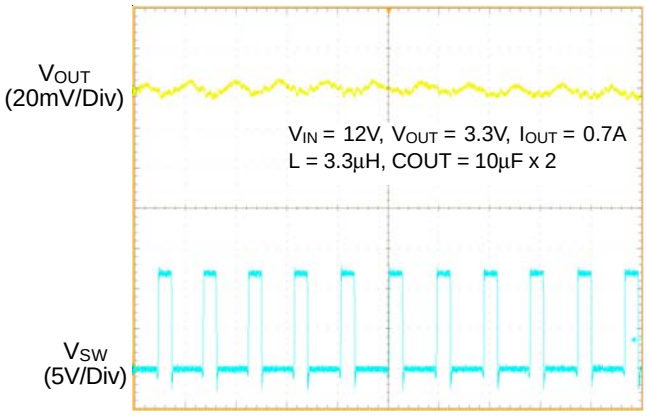
Output Voltage vs. Temperature



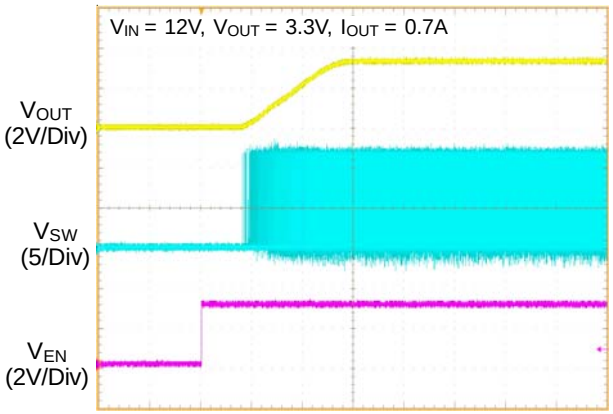
Load Transient Response



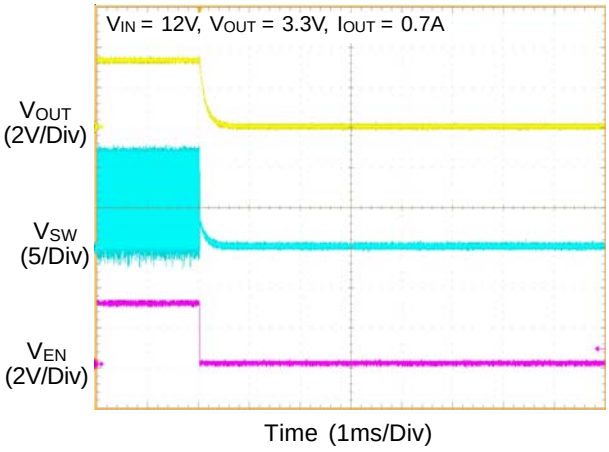
Output Ripple Voltage



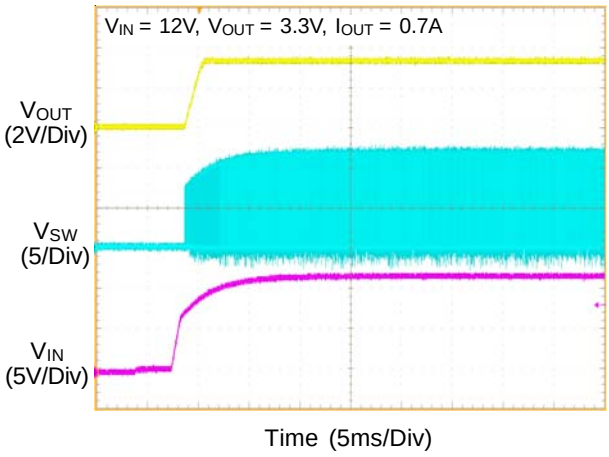
Power On from EN



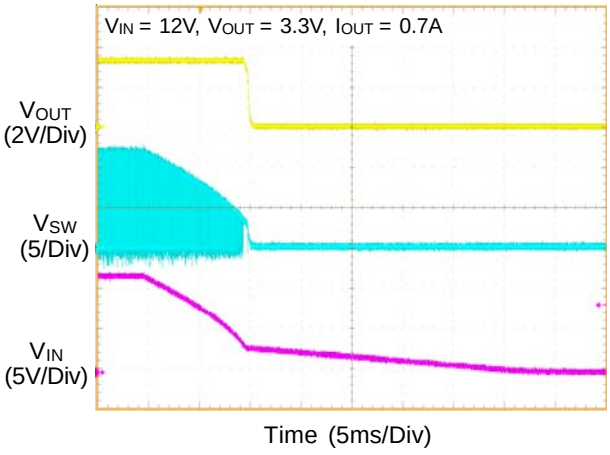
Power Off from EN



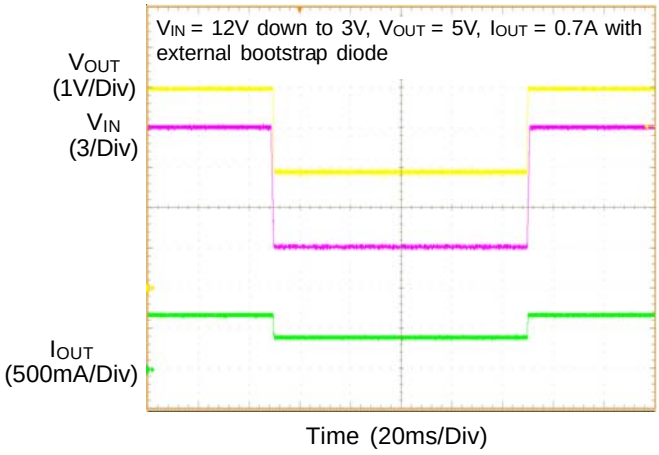
Power On from VIN



Power Off from VIN



Momentary Drop



Application Information

The output stage of a synchronous buck converter is composed of an inductor and capacitor, which stores and delivers energy to the load, and forms a second-order low-pass filter to smooth out the switch node voltage to maintain a regulated output voltage. The output voltage can be up to 28V at proper operation condition.

Output Voltage Setting

For the RTQ2130B, there are two output voltage setting options: one is that trimmed output voltage options for a fixed output voltage are available for the VS pin, and the other is through a resistive divider to sense a fraction of the output voltage at the FB pin as shown in Figure 3.

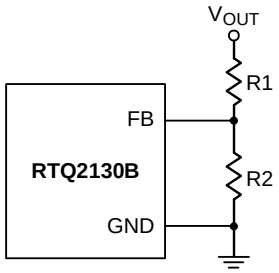


Figure 3. Output Voltage Setting

The output voltage is set by the external resistive voltage divider, and can be calculated by the following equation :

$$V_{OUT} = 0.8V \times \left(1 + \frac{R1}{R2}\right)$$

External Bootstrap Diode

Connect a 0.1µF low-ESR ceramic capacitor between the BOOT and SW pins. This capacitor provides the supply voltage for the high-side MOSFET gate driver. It is recommended to add an external bootstrap diode from an external 5V supply voltage to the BOOT pin to improve efficiency when the input voltage V_{IN} is lower than 5.5V, or duty cycle is higher than 65%. A low-cost bootstrap diode can be used, such as IN4148 or BAT54. The external 5V supply voltage can be a fixed voltage supply coming from the system, or the 5V output voltage generated in the system. Note that the $V_{BOOT-SW}$ must be lower than 5.5V.

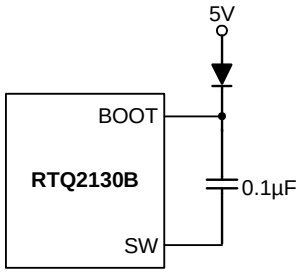


Figure 4. External Bootstrap Diode

Chip Enable Operation

For automatic start-up, the EN pin can be connected to VIN, directly. The inherent hysteresis makes EN useful as a simple time delay. To add an additional time delay, the EN pin can be connected to VIN through a resistor R_{EN} and to GND through a capacitor C_{EN}, as shown in Figure 5. The additional time delay for switching operation to start can be calculated with the EN's internal logic threshold, 1.45V (typ.).

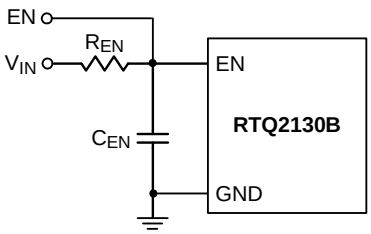


Figure 5. Enable Timing Control

An external MOSFET can be added to implement an logic-controlled EN pin, as shown in Figure 6. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 can provide the logic control on the EN pin, pulling it down.

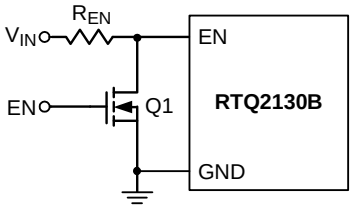


Figure 6. Digital Enable Control Circuit

Under-Voltage Protection

The RTQ2130B provides under-voltage protection (UVP) with hiccup mode. When the FB voltage drops below 50% of the reference voltage V_{REF}, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RTQ2130B will automatically attempt to restart. When the UVP condition is removed, the converter will resume normal operation. The UVP is disabled during soft-start.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency can determine the inductor ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A lower inductor ripple current reduces not only ESR losses in output capacitors but also output ripple voltage. Higher efficiency operation can be achieved at higher frequency with smaller ripple current. This, however, requires a larger inductor.

For the ripple current selection, the value of ΔI_L, which is IMAX multiplied by 0.3 will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left(\frac{V_{OUT}}{f_{SW} \times \Delta I_{L(MAX)}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

To ensure the converter can operate properly, the maximum inductor peak current must always meet the inductor saturation current rating and temperature rating.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low-ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current equation is given as below :

$$I_{RMS} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2 x V_{OUT}, where I_{RMS} = I_{OUT} / 2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, two 10µF low-ESR ceramic capacitors are suggested.

The selection of C_{OUT} is determined by the required ESR to minimize the ripple voltage. Moreover, the bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple voltage, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 \times fsw \times C_{OUT}}\right)$$

The highest output ripple voltage will be at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Ceramic capacitors of larger capacitance and lower cost are now available in smaller case sizes. The high ripple current, and voltage ratings, and low-ESR characteristics of such capacitors make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power supply is from a wall adapter through a long wire, the ceramic capacitor and the wire inductance can result in significant input voltage ringing, triggered by a load step at the output. At best, this ringing will be coupled to the output and be mistaken as loop instability. At worst, an inrush current through the long wire may cause a large voltage spike at VIN to damage the converter.

Compensation Network Design

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operations. Typical symptoms of an unstable power supply include: audible noise from the magnetic components or

ceramic capacitors, jittering in the switching waveforms, oscillation of output voltage, overheating of power FETs and so on.

In most cases, the peak current mode control architecture used in the RTQ2130B only requires two external components to achieve a stable design as shown in Figure 7. The compensation can be selected to accommodate any capacitor type or value. The external compensation also allows the user to set the crossover frequency and optimize the transient performance of the device. Around the crossover frequency the peak current mode control (PCMC) equivalent circuit of Buck converter can be simplified as shown in Figure 8. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Since the slope compensation is ignored, the actual cross over frequency will usually be lower than the crossover frequency used in the calculations. It is always necessary to make a measurement before releasing the design for final production. Though the models of power supplies are theoretically correct, they cannot take full account of circuit parasitic and component nonlinearity, such as the ESR variations of output capacitors, then on linearity of inductors and capacitors, etc. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. A Bode plot is ideally measured with a network analyzer while RICHTEK application note AN038 provides an alternative way to check the stability quickly and easily. Generally, follow the following steps to calculate the compensation components :

1. Set up the crossover frequency, f_C. For stability purposes, our target is to have a loop gain slope that is –20dB/decade from a very low frequency to beyond the crossover frequency. Do "NOT" design the crossover frequency over 90kHz with the RTQ2130B. For dynamic purposes, the higher the bandwidth, the faster the load transient response. The downside to high bandwidth is that it increases the regulators susceptibility to board noise which ultimately leads to excessive falling edge jitter of the switch node voltage.

2. R_{COMP} can be determined by :

$$R_{COMP} = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{gm \times V_{REF} \times gm\_cs} = \frac{2\pi \times f_C \times C_{OUT}}{gm \times gm\_cs} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}}$$

where

gm is the error amplifier gain of trans-conductance (950μA/V)

gm_cs is COMP to current sense (1.2 A/V)

3. A compensation zero can be placed at or before the dominant pole of buck which is provided by output capacitor and maximum output loading(R_L). Calculate C_{COMP} :

$$C_{COMP} = \frac{R_L \times C_{OUT}}{R_{COMP}}$$

Output capacitor and its ESR provide a zero and optional C_{COMP2} can be used to cancel this zero

$$C_{COMP2} = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}}$$

Note : Generally, C_{COMP2} is not necessary for the output using ceramic capacitor due to the ESR is extremely low.

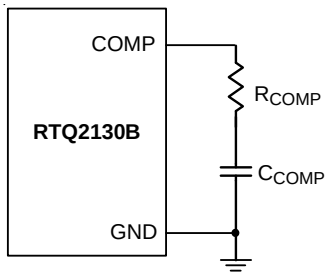


Figure 7. External Compensation Components

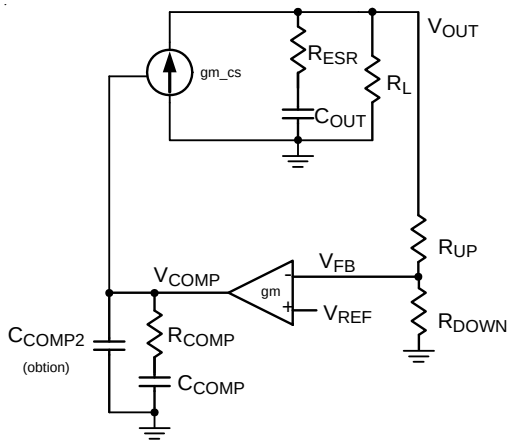


Figure 8. Simplified Equivalent Circuit of Buck with PCMC

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-8SL 2x3 package, the thermal resistance, θ_{JA}, is 41°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (150°C – 25°C) / (41°C/W) = 3.05W for a WDFN-8SL 2x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

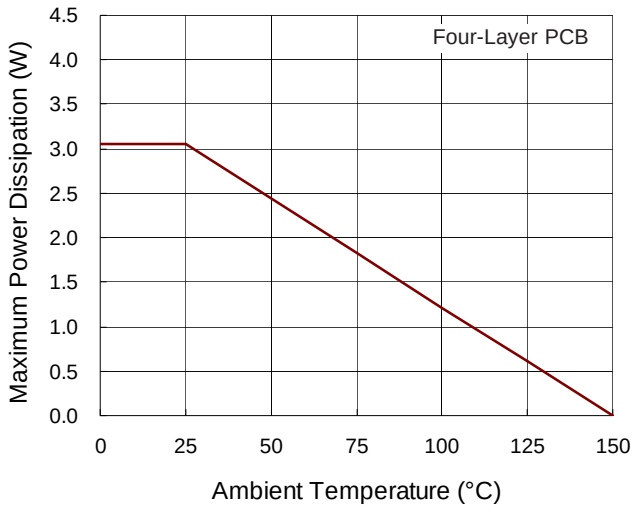
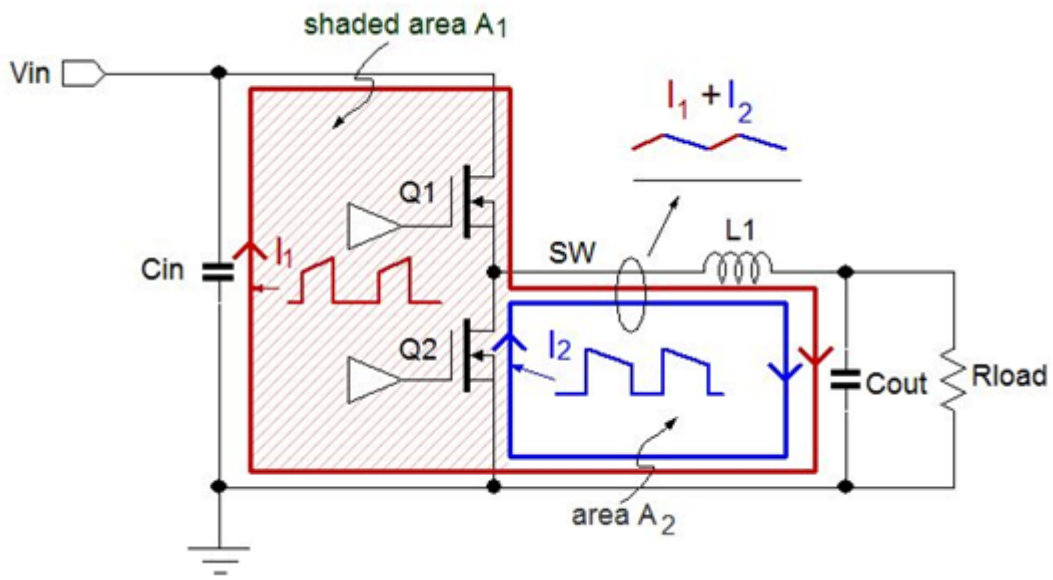


Figure 9. Derating Curve of Maximum Power Dissipation

Layout Considerations

The below figure shows the two main loops in the buck converter, where the shaded loop with area A_1 is the most critical loop because the current I_1 in this loop consists of discontinuous current pulses with high dI/dt. Since radiation is proportional to the loop area, it is most important to make the loop area A_1 as small as possible. Loop area A_2 is less critical, because the current in this loop ($I_1 + I_2$) is a continuous triangle shaped waveform with much lower dI/dt than I_1.



Follow the PCB layout guidelines for optimal performance of the device.

- Keep the traces of the input and output current paths as short and wide as possible. To keep small main loop area, C_{IN} → IC_VIN → IC_SW → Inductor(L1) → C_{OUT} → GND.
- To minimize area A1 in the layout, the input capacitors should be placed as close as possible to the IC, and make a short connection with IC VIN and GND.
- Place high frequency decoupling capacitor CIN1 as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- To further reduce loop impedance, the input current return path should be placed underneath the input capacitors and let the return path overlap the top input power line to get small AC return path.
- To minimize distance between the layer of main power loop to layer of current return path to get small AC return path. Minimizing the parasitic loop impedance will minimize switch node ringing and EMI.
- SW node is with high frequency voltage swing and should be connected to inductor by short trace.
- BOOT node is with high frequency voltage swing and place C_{BOOT} capacitor with smallest parasitic loop.
- Keep analog components away from the SW and BOOT node to prevent stray capacitive noise pickup and minimize EMI.
- Connect feedback network behind the output capacitors.
- Place the feedback components near the device.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- Vias must be placed to inner ground layers to help reduce ground impedance and to serve as heat removal from the IC thermal pad.
- Place capacitor for VCC and should be placed as close as possible to the IC.
- The example of the RTQ2130B PCB layout guide are shown as below

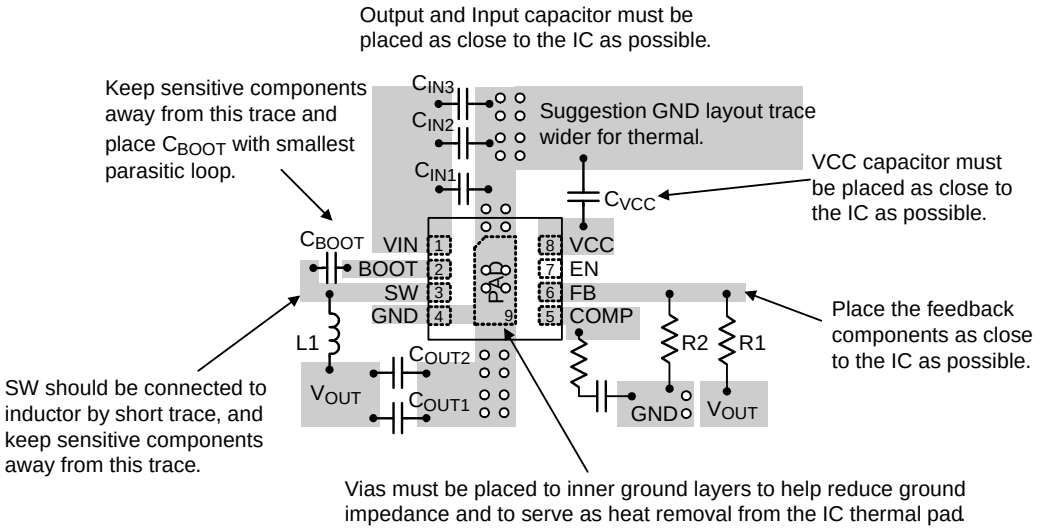
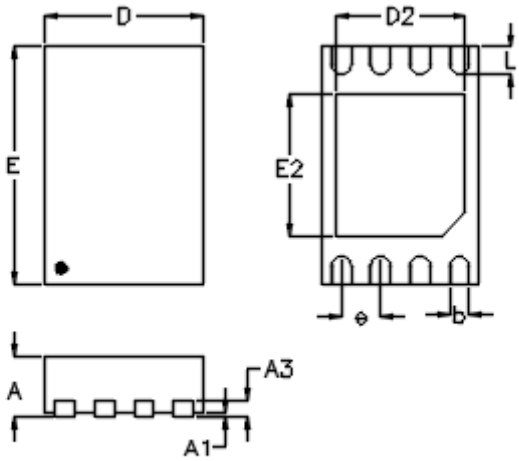
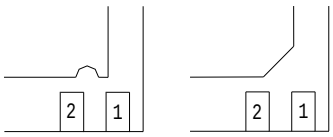


Figure 10. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.900	2.100	0.075	0.083
D2	1.600	1.700	0.063	0.067
E	2.900	3.100	0.114	0.122
E2	1.750	1.850	0.069	0.073
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8SL DFN 2x3 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789