



Z86E61 AND Z86E63

CMOS Z8® OTP MICROCONTROLLER

GENERAL DESCRIPTION

The Z86E61 is a member of the Z8® single-chip microcontroller family with 16 Kbytes of EPROM and 236 bytes of general-purpose RAM and the Z86E63 has 32K bytes of EPROM.

The Z86E61/63 are pin compatible, One-Time-Programmable (OTP) versions of the Z86C61/63. The Z86E61/63 contain 16/32 Kbytes of EPROM memory in place of the 16/32 Kbytes of ROM on the Z86C61/63.

The MCU is housed in a 40-pin DIP, 44-pin Leaded Chip-Carrier, or a 44-pin Quad Flat Pack, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. The MCU can address both external memory and preprogrammed ROM which enables this Z8 microcomputer to be used in high volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E61/63 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86E61/63 fulfills this with 32-pin dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory and 236 general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the Z86E61/63 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Functional Block description).

Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power Ground	V _{CC} GND	V _{DD} V _{SS}

PRODUCT RECOMMENDATIONS

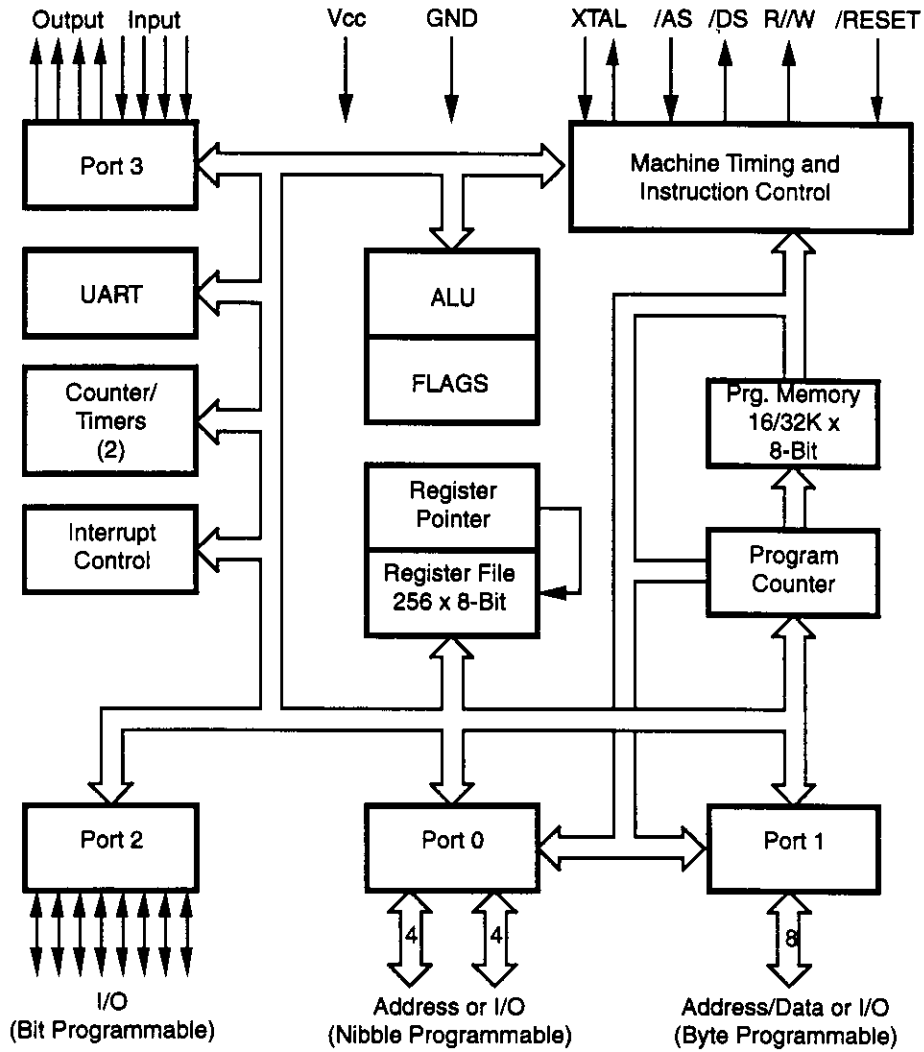
Zilog recommends the following programming equipment for use with this One-Time-Programmable product:

Device	Zilog Support Tool	Recommended Revision Level	
		Hardware	Software
Z86E61/63	Z86C1200ZEM ICEBOX™ Emulator* (*Does not support 4K/8K option.)	B	2.1

Some non-Zilog programmers may have different programming waveforms, voltages and timings and not all programmers may meet the programming requirements of Zilog's One-Time-Programmable products.

If difficulty is encountered in programming a Zilog OTP product, please contact your local Zilog sales office.

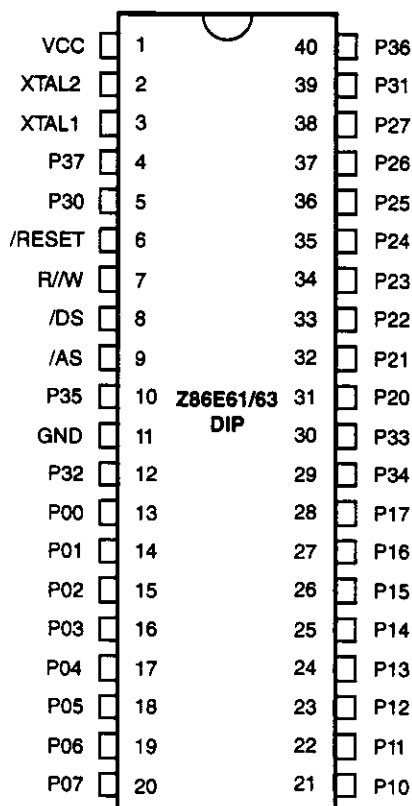
GENERAL DESCRIPTION (Continued)



Functional Block Diagram

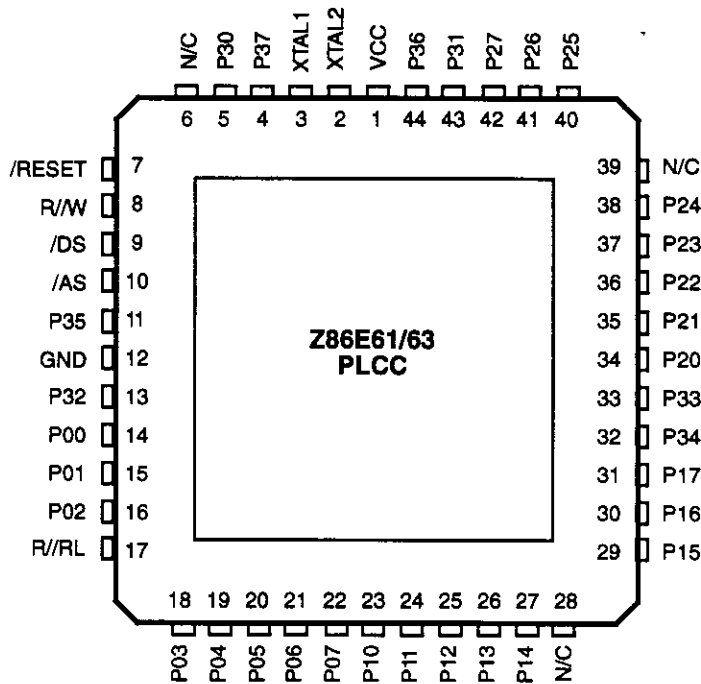
PIN DESCRIPTION

Standard Mode


40-Lead DIP Pin Assignments
40-Lead DIP Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input	11	GND	Ground, GND	Input
2	XTAL2	Crystal, Oscillator Clock	Output	12	P32	Port 3 Pin 2	Input
3	XTAL1	Crystal, Oscillator Clock	Input	13-20	P00-P07	Port 0 Pins 0,1,2,3,4,5,6,7	In/Output
4	P37	Port 3 Pin 7	Output	21-28	P10-P17	Port 1 Pins 0,1,2,3,4,5,6,7	In/Output
5	P30	Port 3 Pin 0	Input	29	P34	Port 3 Pin 4	Output
6	/RESET	Reset	Input	30	P33	Port 3 Pin 3	Input
7	R/W	Read/Write	Output	31-38	P20-P27	Port 2 Pins 0,1,2,3,4,5,6,7	In/Output
8	/DS	Data Strobe	Output	39	P31	Port 3 Pin 1	Input
9	/AS	Address Strobe	Output	40	P36	Port 3 Pin 6	Output
10	P35	Port 3 Pin 5	Output				

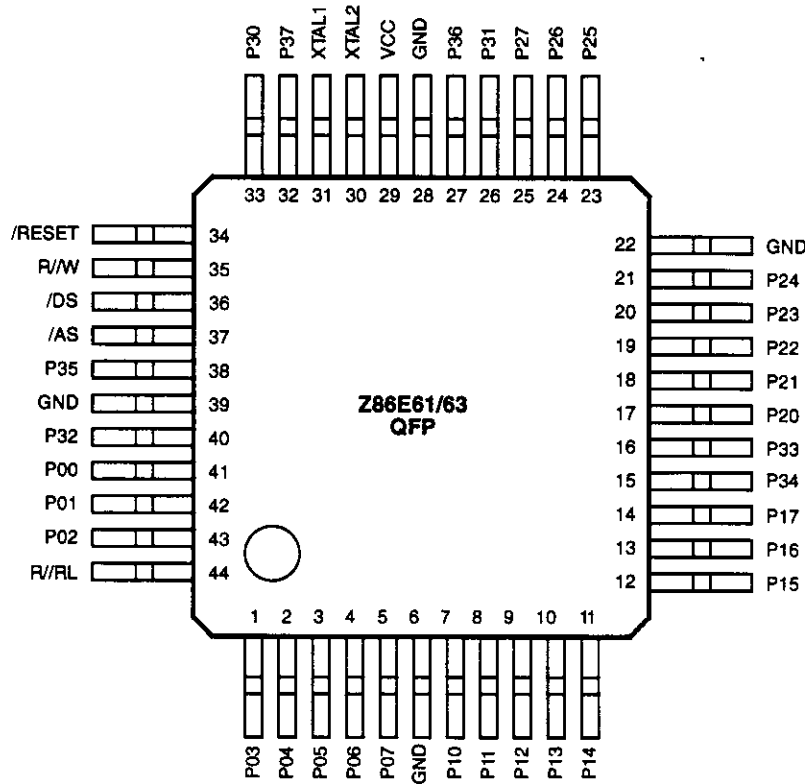
PIN DESCRIPTION (Continued)
Standard Mode



44-Lead PLCC Pin Assignments

44-Lead PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input	14-16	P00-P02	Port 0 Pins 0,1,2	In/Output
2	XTAL2	Crystal, Oscillator Clock	Output	17	R//RL	ROM/ROMless control	Input
3	XTAL1	Crystal, Oscillator Clock	Input	18-22	P03-P07	Port 0 Pins 3,4,5,6,7	In/Output
4	P37	Port 3 pin 7	Output	23-27	P10-P14	Port 1 Pins 0,1,2,3,4	In/Output
5	P30	Port 3 Pin 0	Input	28	N/C	Not Connected	Input
6	N/C	Not Connected	Input	29-31	P15-P17	Port 1 Pins 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3 Pin 4	Output
8	R/W	Read/Write	Output	33	P33	Port 3 Pin 3	Input
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2 Pins 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected	Input
11	P35	Port 3 Pin 5	Output	40-42	P25-P27	Port 2 Pins 5,6,7	In/Output
12	GND	Ground, GND	Input	43	P31	Port 3 Pin 1	Input
13	P32	Port 3 Pin 2	Input	44	P36	Port 3 Pin 6	Output



44-Lead QFP Pin Assignments

44-Lead QFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0 Pins 3,4,5,6,7	In/Output
6	GND	Ground, GND	Input
7-14	P10-P17	Port 1 Pins 0,1,2,3,4,5,6,7	In/Output
15	P34	Port 3 Pin 4	Output
16	P33	Port 3 Pin 3	Input
17-21	P20-P24	Port 2 Pins 0,1,2,3,4	In/Output
22	GND	Ground, GND	Input
23-25	P25-P27	Port 2 Pins 5,6,7	In/Output
26	P31	Port 3 Pin 1	Input
27	P36	Port 3 Pin 6	Output
28	GND	Ground, GND	Input
29	V _{cc}	Power Supply	Input
30	XTAL2	Crystal, Oscillator Clock	Output

Pin #	Symbol	Function	Direction
31	XTAL1	Crystal, Oscillator Clock	Input
32	P37	Port 3 Pin 7	Output
33	P30	Port 3 Pin 0	Input
34	/RESET	Reset	Input
35	R/W	Read/Write	Output
36	/DS	Data Strobe	Output
37	/AS	Address Strobe	Output
38	P35	Port 3 Pin 5	Output
39	GND	Ground, GND	Input
40	P32	Port 3 Pin 2	Input
41-43	P00-P02	Port 0 Pins 0,1,2	In/Output
44	R//RL	ROM/ROMless control	Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp		†	C

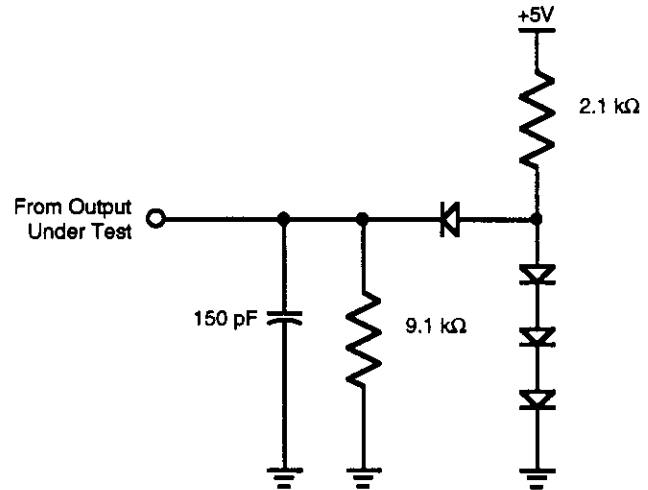
Notes:

- * Voltages on all pins with respect to GND.
13.0 V Maximum on P30-P33.
- † See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

SPECIAL NOTE

- 1) V_{CC} operation range is 4.5V to 5.5V.
- 2) High voltage (VH) programming voltage for V_{pp} , /CE, /EPM, and /OE pins is $12.0 \pm 0.5V$ when in OTP mode.
- 3) Programming temperature is 20°C to 30°C.
- 4) Minimum operating frequency is 2.5 MHz.

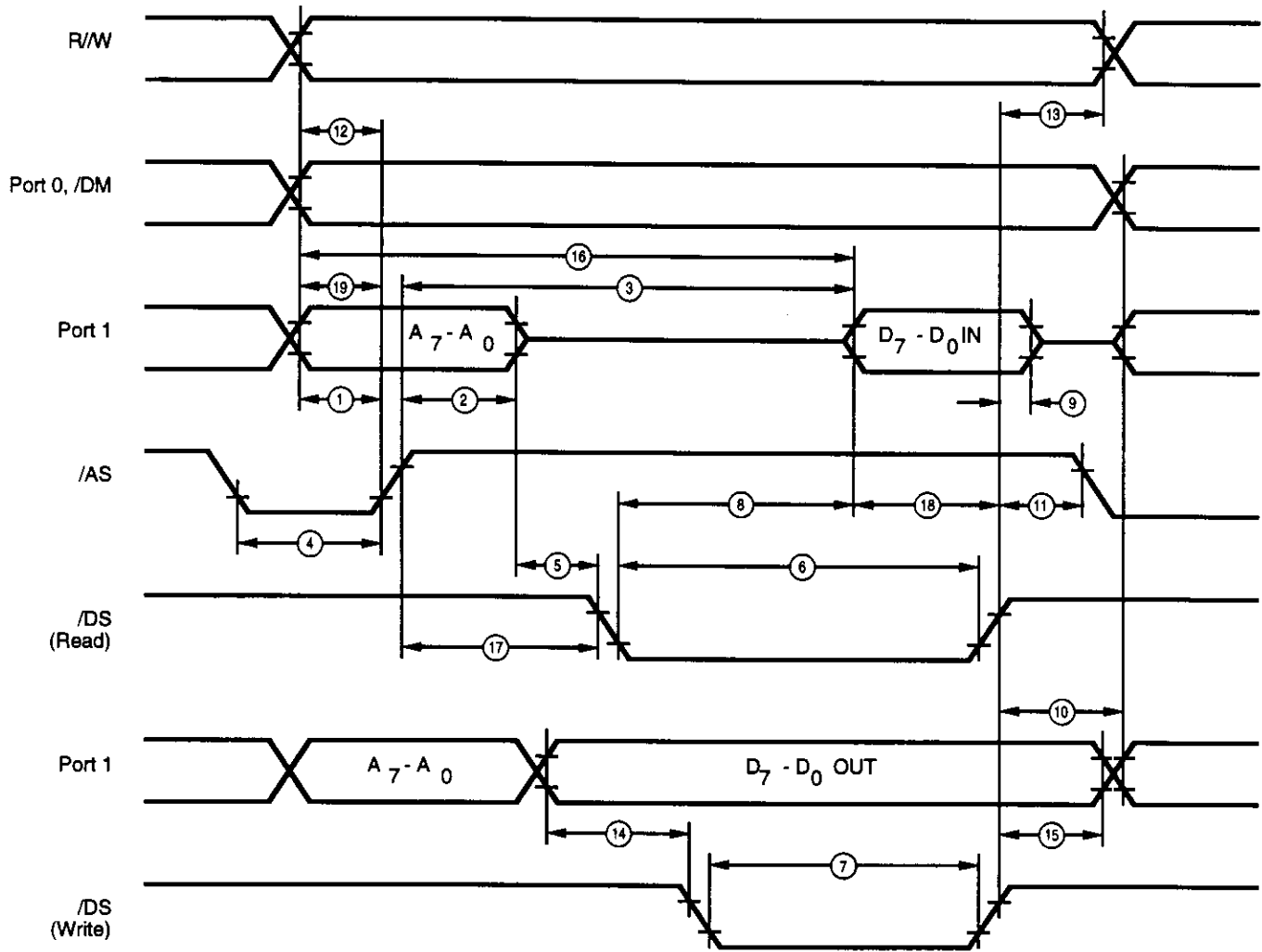
DC CHARACTERISTICS

VCC = 4.5V to 5.5V

Sym	Parameter	$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		Typical at 25°C	Units	Conditions
		Min	Max			
	Max Input Voltage		7		V	$I_{IN} < 250 \mu\text{A}$
	Max Input Voltage		12.5V		V	P30-P33 Only in OTP mode
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -2.0 \text{ mA}$
V_{OL}	Output Low Voltage		0.4		V	$I_{OL} = +2.0 \text{ mA}$
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.3	0.8		V	
I_{IL}	Input Leakage	-10	10		μA	$0\text{V} < V_{IN} < +5.25\text{V}$
I_{OL}	Output Leakage	-10	10		μA	$0\text{V} < V_{IN} < +5.25\text{V}$
I_{IR}	Reset Input Current		-50		μA	$V_{CC} = +5.25\text{V}, V_{RL} = 0\text{V}$
I_{CC}	Supply Current		50	25	mA	@ 12 MHz
			60	35	mA	@ 16 MHz
I_{CC1}	Standby Current		15	5	mA	HALT Mode $V_{IN} = 0\text{V}, V_{CC}$ @ 12 MHz
			20	10	mA	HALT Mode $V_{IN} = 0\text{V}, V_{CC}$ @ 16 MHz
I_{CC2}	Standby Current		20	5	μA	STOP Mode $V_{IN} = 0\text{V}, V_{CC}$ @ 12 MHz
			20	5	μA	STOP Mode $V_{IN} = 0\text{V}, V_{CC}$ @ 16MHz

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

VCC = 4.5V to 5.5V

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$				Units	Notes
			12 MHz		16 MHz			
			Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS Rise Delay	35		20		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		30		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		220		180	ns	[1,2,3]
4	TwAS	/AS Low Width	55		35		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	45		35		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	55		30		ns	[2,3]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	30		20		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	35		30		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	35		30		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		255		200	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	55		40		ns	[2,3]
18	TdDI(DS)	Data Input Setup to /DS Rise	75		60		ns	[1,2,3]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	50		30		ns	[2,3]

Notes:

- [1] When using extended memory timing add 2 TpC.
 [2] Timing numbers given are for minimum TpC.
 [3] See clock cycle dependent characteristics table.

Standard Test Load

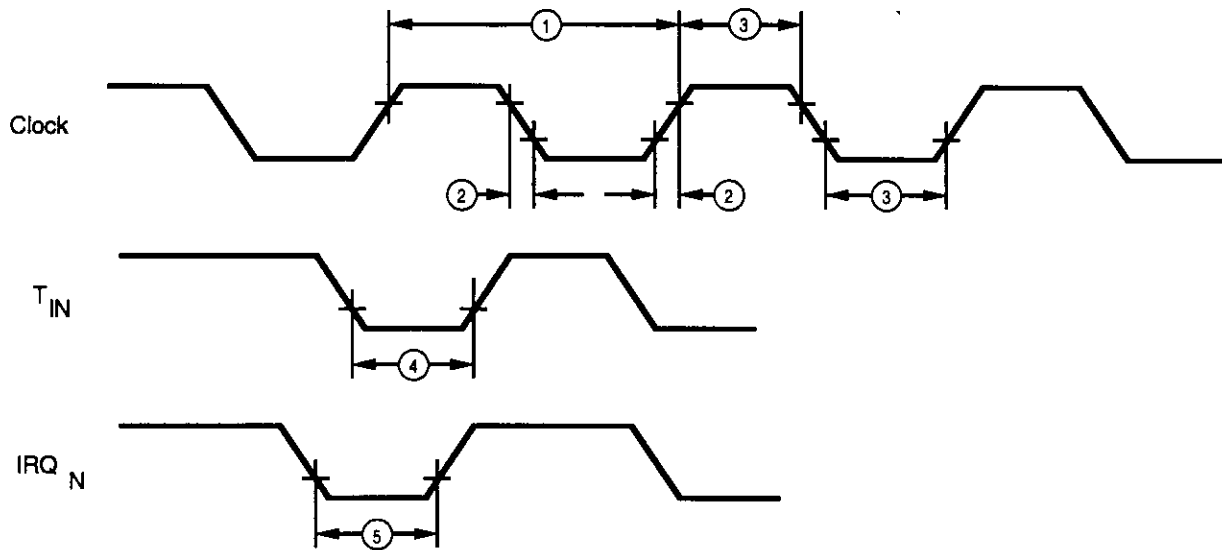
All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	$0.40T_{pC} + 0.32$
2	TdAS(A)	$0.59T_{pC} - 3.25$
3	TdAS(DR)	$2.38T_{pC} + 6.14$
4	TwAS	$0.66T_{pC} - 1.65$
6	TwDSR	$2.33T_{pC} - 10.56$
7	TwDSW	$1.27T_{pC} + 1.67$
8	TdDSR(DR)	$1.97T_{pC} - 42.5$
10	TdDS(A)	$0.8T_{pC}$
11	TdDS(AS)	$0.59T_{pC} - 3.14$
12	TdR/W(AS)	$0.4T_{pC}$
13	TdDS(R/W)	$0.8T_{pC} - 15$
14	TdDW(DSW)	$0.4T_{pC}$
15	TdDS(DW)	$0.88T_{pC} - 19$
16	TdA(DR)	$4T_{pC} - 20$
17	TdAS(DS)	$0.91T_{pC} - 10.7$
18	TsDI(DS)	$0.8T_{pC} - 10$
19	TdDM(AS)	$0.9T_{pC} - 26.3$

AC CHARACTERISTICS

Additional Timing Diagram



Additional Timing

AC CHARACTERISTICS

Additional Timing Table

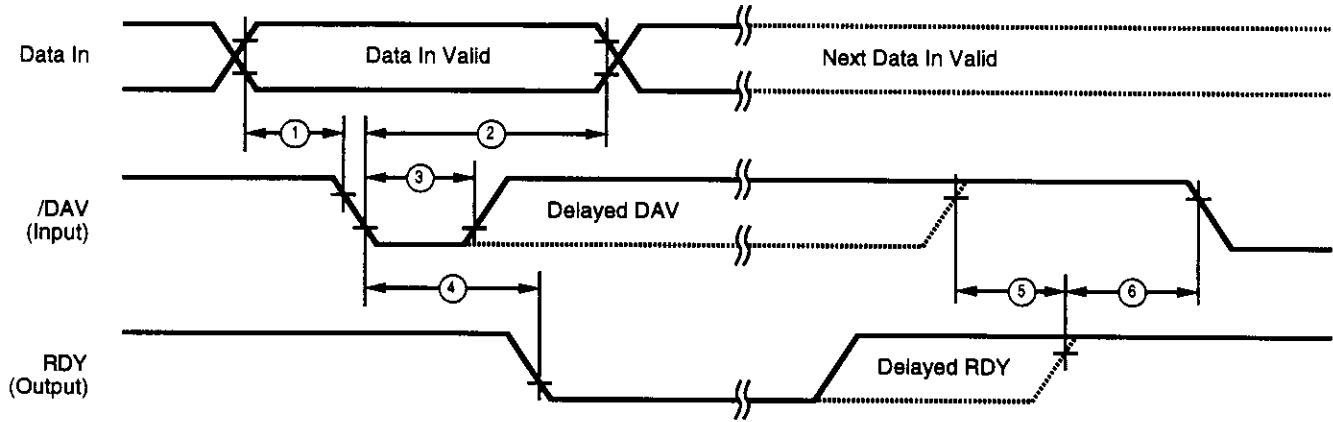
VCC = 4.5V to 5.5V

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$				Units	Notes
			12 MHz	16 MHz	Min	Max		
1	TpC	Input Clock Period	83	500	62.5	500	ns	[1]
2	TrC, TFC	Clock Input Rise & Fall Times		15		10	ns	[1]
3	TwC	Input Clock Width	41		31		ns	[1]
4	TwTinL	Timer Input Low Width	75		50		ns	[2]
5	TwTinH	Timer Input High Width	5TpC		5TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC			[2]
7	TrTin, Tftin	Timer Input Rise & Fall Times	100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	5TpC		5TpC			[2,3]

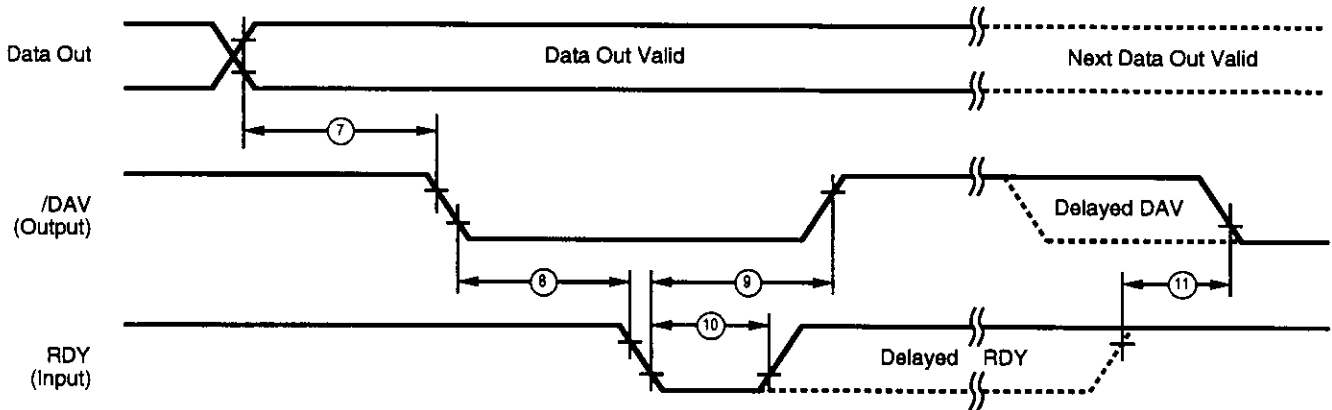
Notes:

- [1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- [2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- [3] Interrupt references request via Port 3.
- [4] Interrupt request via Port 3 (P31-P33).
- [5] Interrupt request via Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing Table

VCC = 4.5V to 5.5V

No	Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$				Notes Data Direction
			12 MHz		16 MHz		
			Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay		TpC		TpC	OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115	OUT

Low Margin:

Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability

stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-con-

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